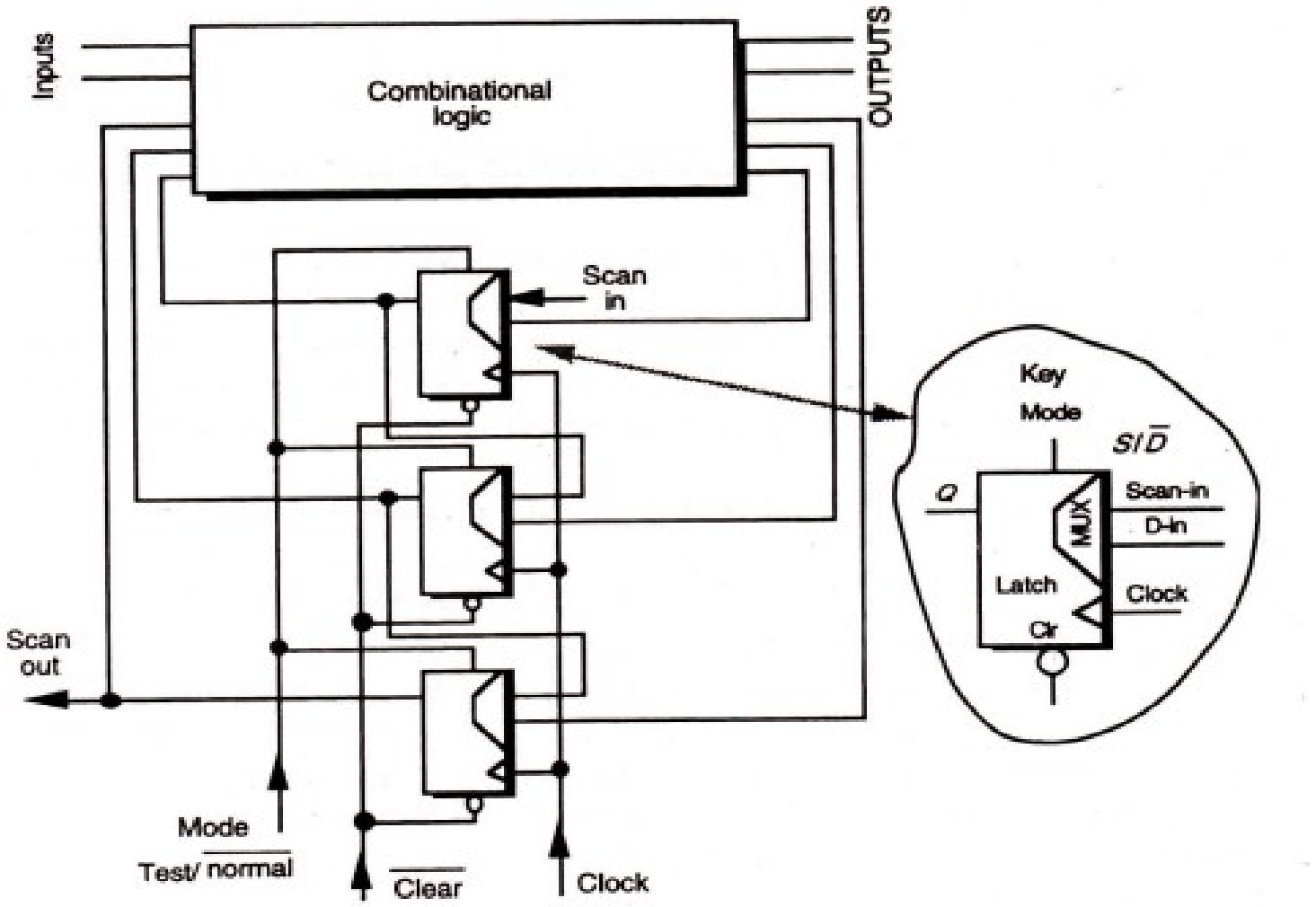
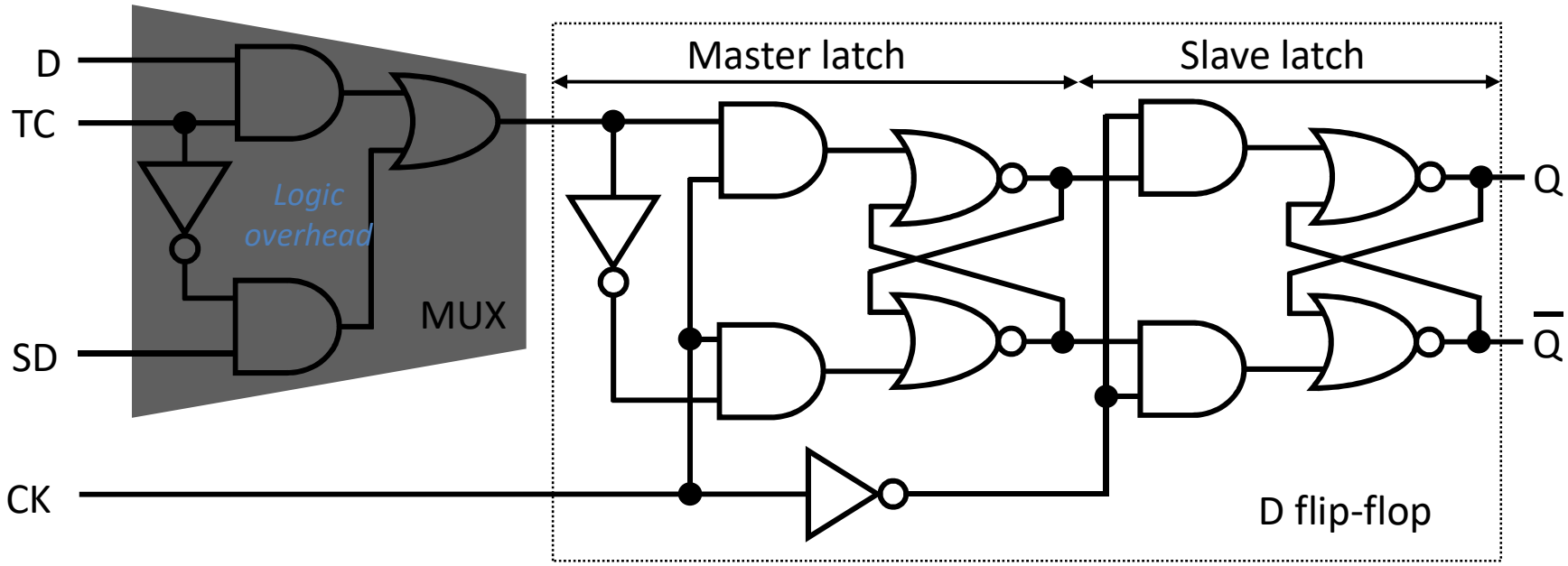
Unit-5

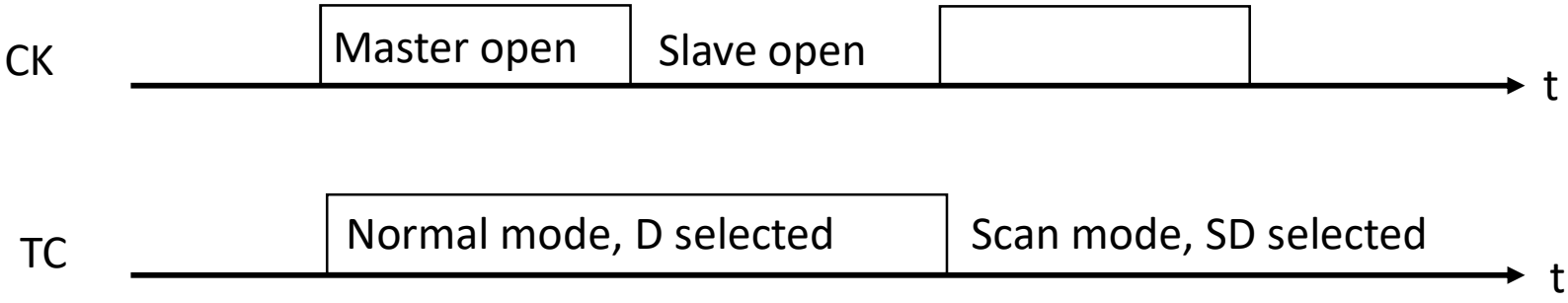
- *Design for testability* (DFT) refers to those design techniques that make test generation and test application cost-effective.
- DFT methods for digital circuits:
  - Ad-hoc methods
  - Structured methods:
    - *Scan*
    - *Partial Scan*
    - *Built-in self-test* (BIST)
    - *Boundary scan*
- DFT method for mixed-signal circuits:
    - Analog test bus

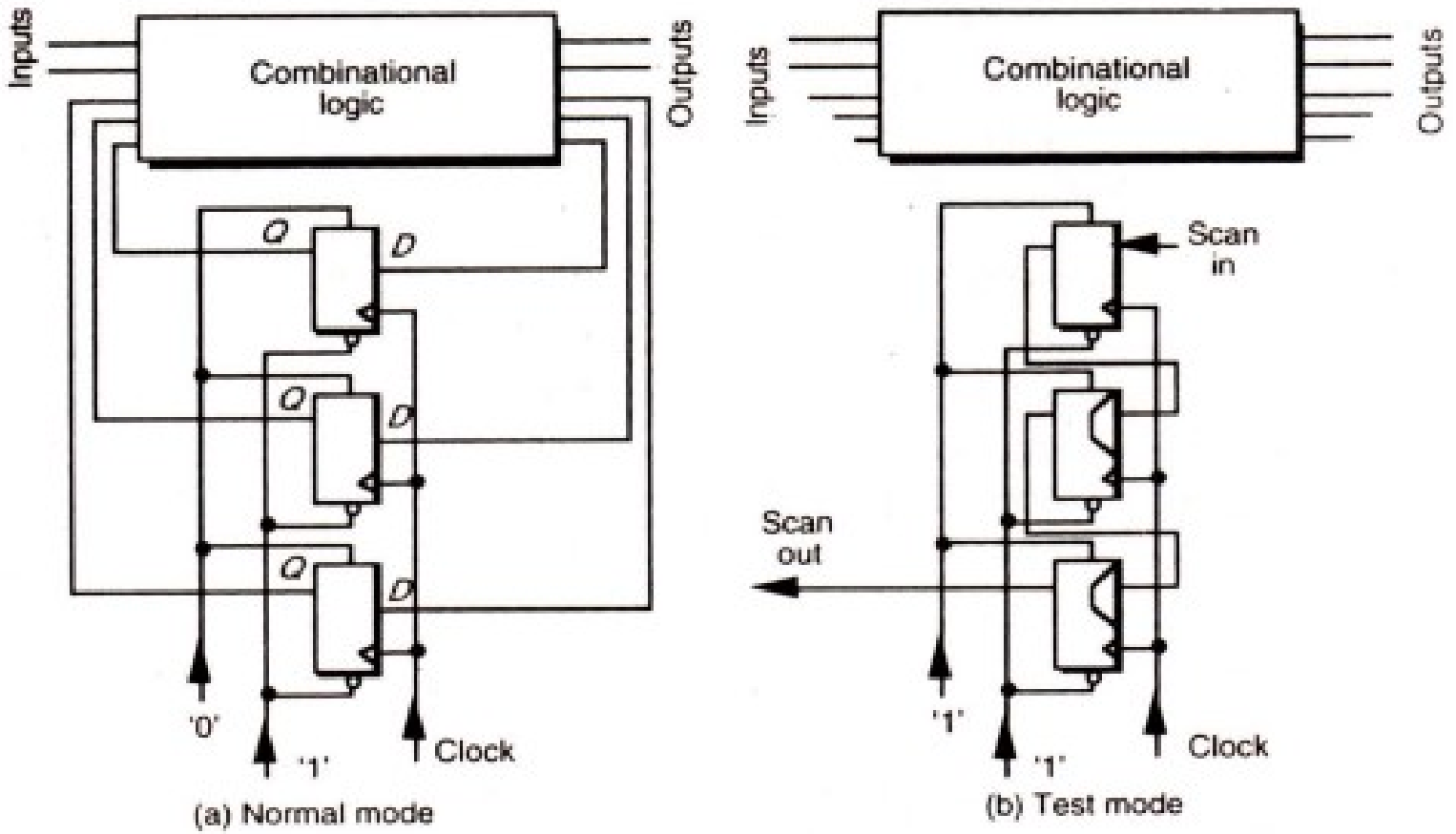
Scan Design Techniques



Scan Flip-Flop (SFF)

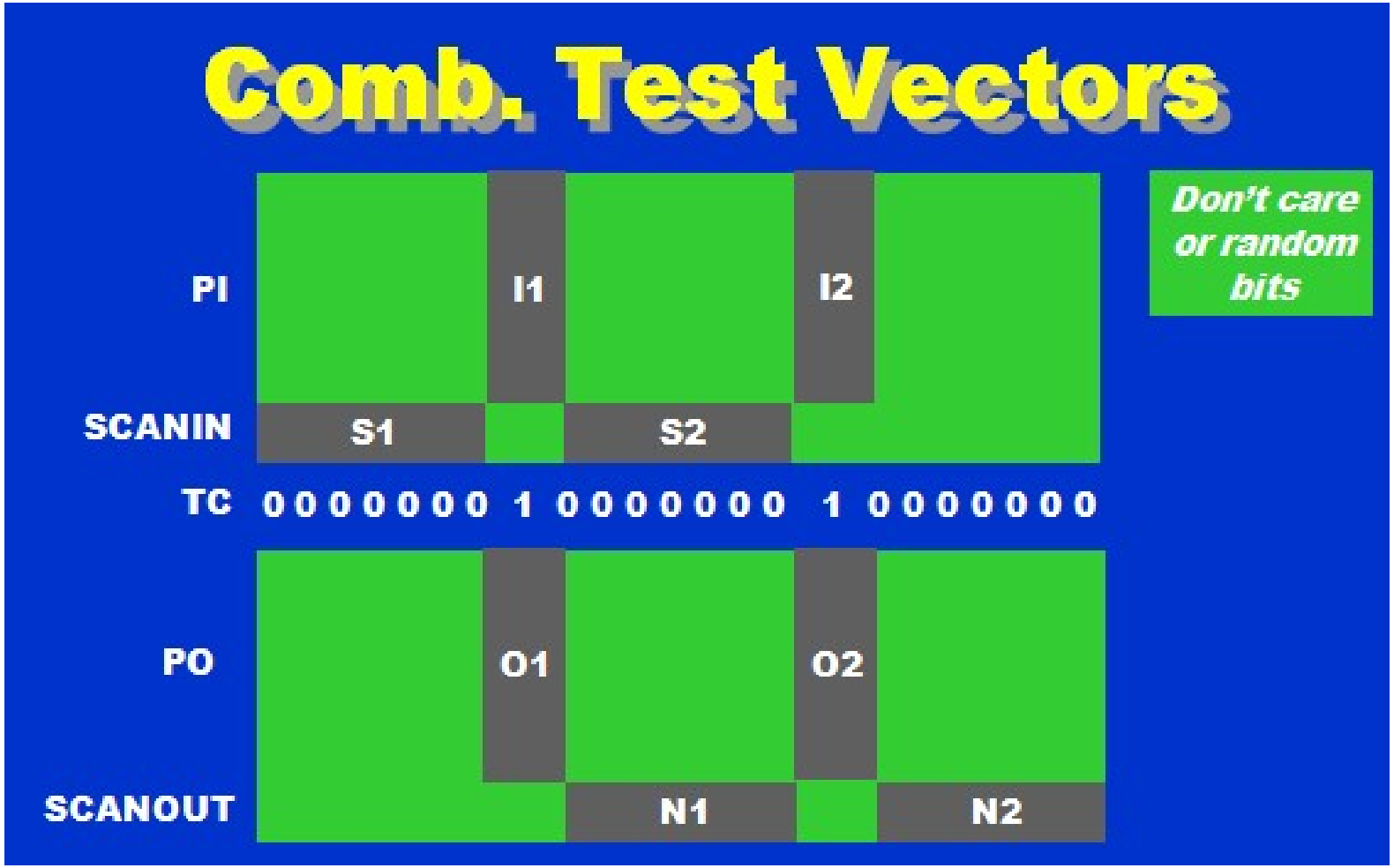




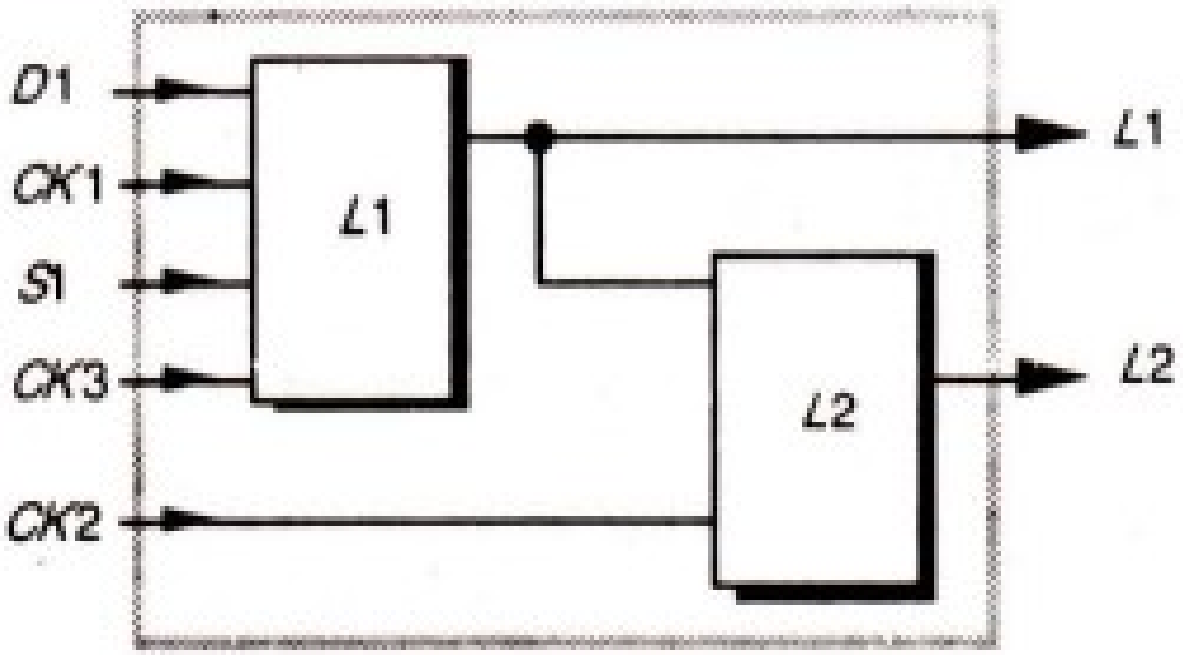


(a) Normal mode

(b) Test mode


Comb. Test Vectors
PI
I1
I2
Don't care or random bits
SCANIN
S1
S2
TC
0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0
PO
O1
O2
SCANOUT
N1
N2

Level-sensitive scan design (LSSD)

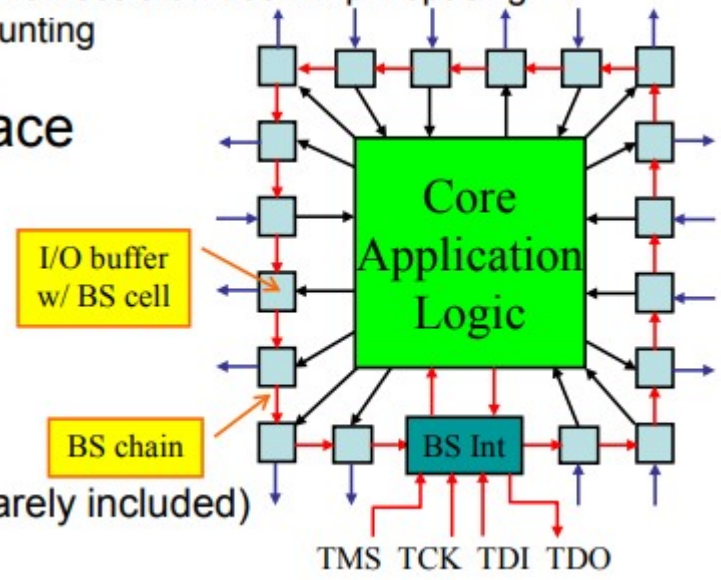


- The ***level-sensitive*** aspect of the method means that a sequential circuit is designed so that the steady-state response to any input state change is independent of the component and wire delays within the circuit.
- Also, if an input state change involves the changing of more than one-input signal, the response must be independent of the order in which they change.
- In LSSD, all internal storage is implemented in ***hazard-free polarity-hold latches***

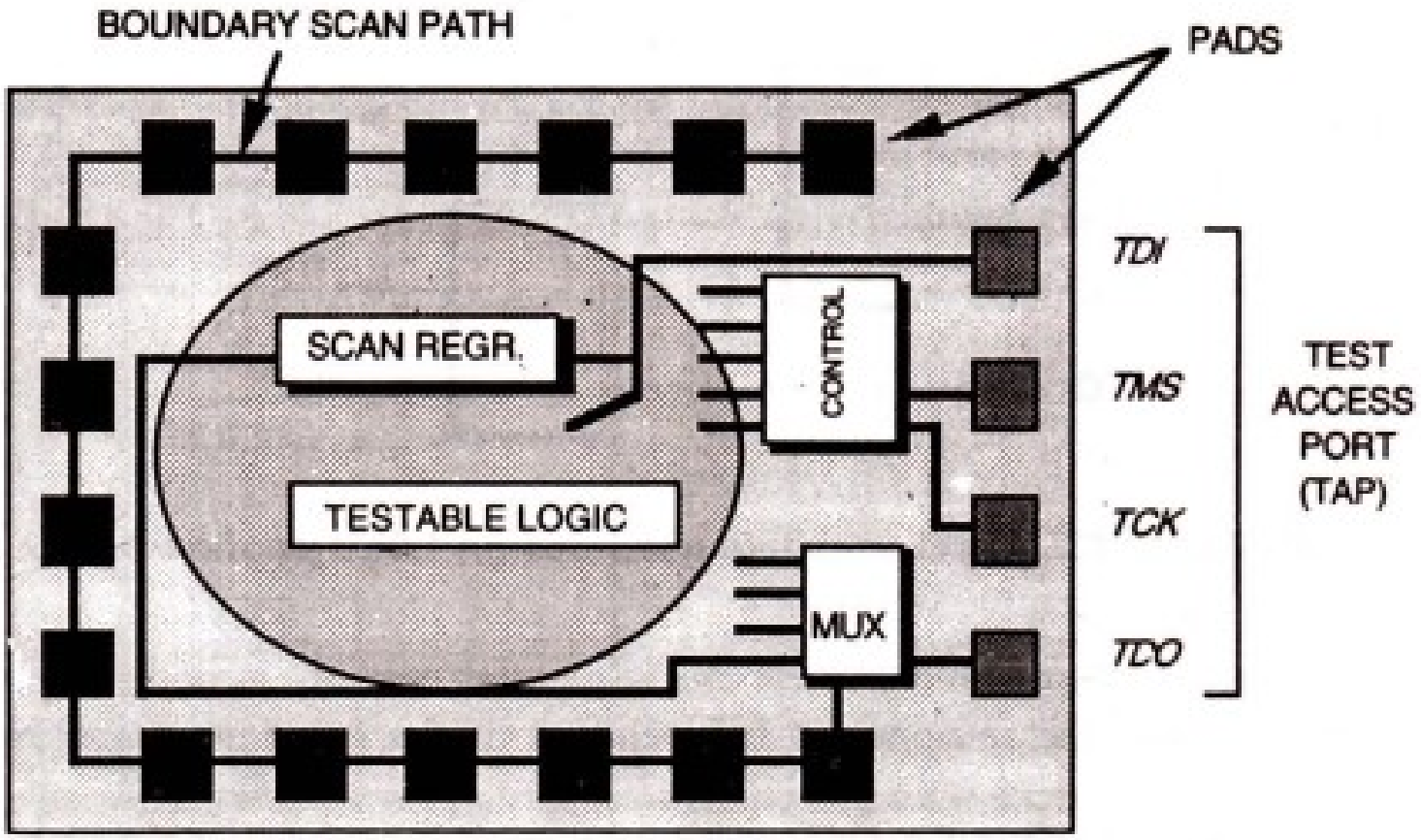
Boundary Scan (BS) IEEE 1149.1 Standard

- Developed for testing chips on a printed circuit board (PCB).
- A chip with BS can be accessed for test from the edge connector of PCB.
- BS hardware added to chip:
  - Test Access port (TAP) added
    - Four test pins
    - A test controller FSM
  - A scan flip-flop added to each I/O pin.
- Standard is also known as JTAG (Joint Test Action Group) standard.

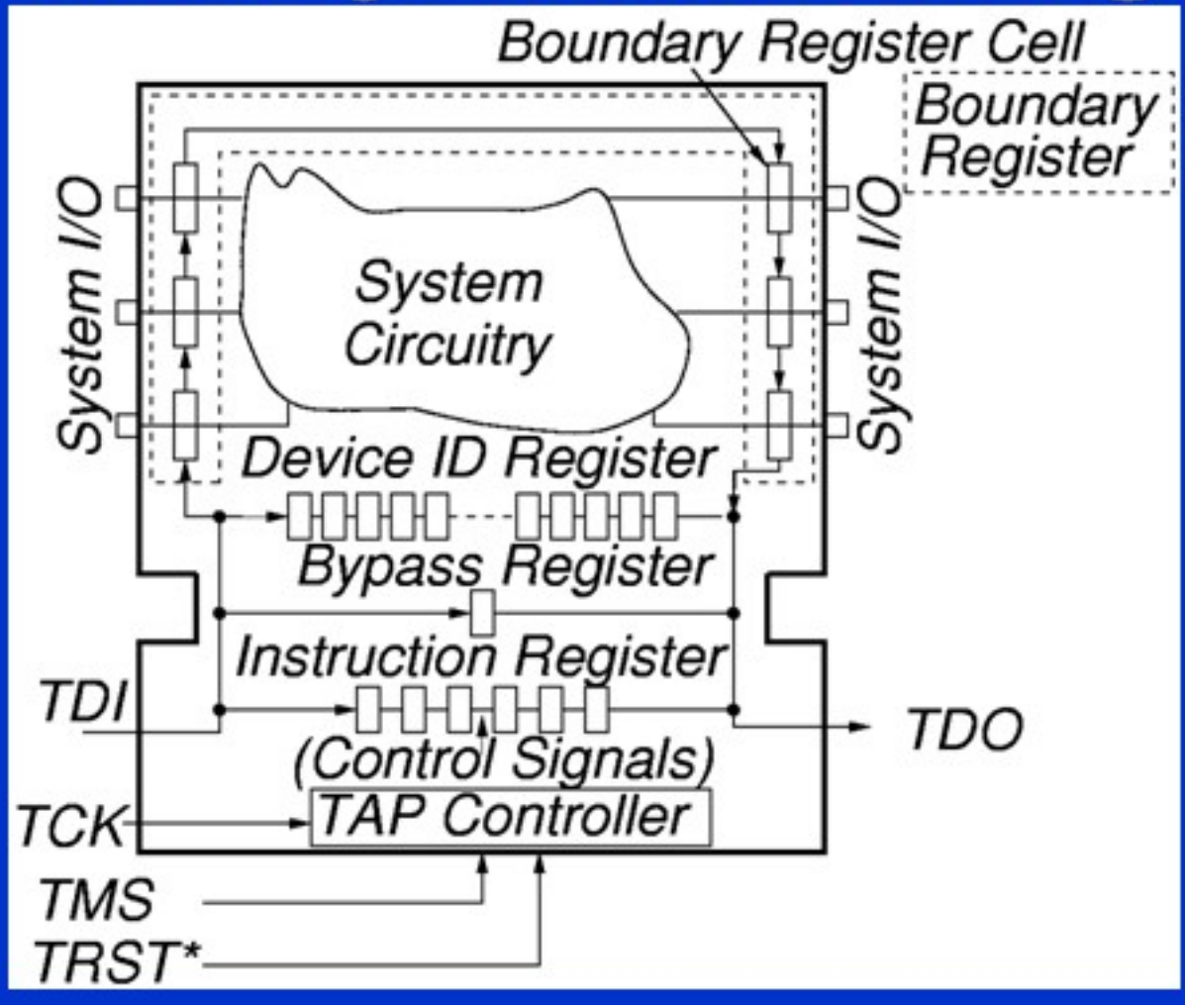
- Developed to test interconnect between chips on PCB
  - Originally referred to as JTAG (Joint Test Action Group)
  - Uses scan design approach to test external interconnect
  - No-contact probe overcomes problem of “in-circuit” test:
    - surface mount components with less than 100 mil pin spacing
    - double-sided component mounting
    - micro- and floating vias
- Standardized test interface
  - IEEE standard 1149.1
  - Four wire interface
    - TMS - Test Mode Select
    - TCK - Test Clock
    - TDI - Test Data In
    - TDO - Test Data Out
    - TRST - reset (optional & rarely included)



Boundary scan test (BST)

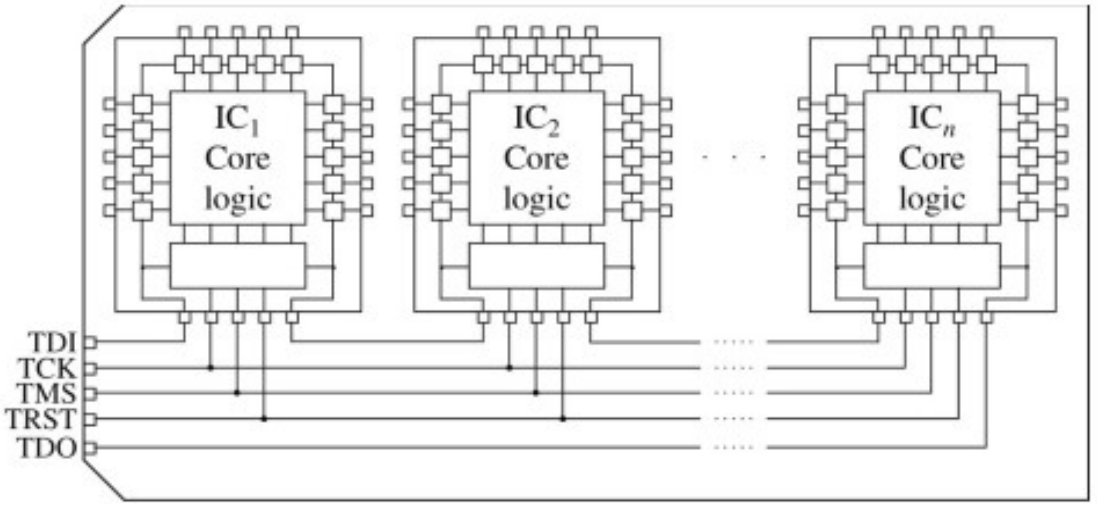


Boundary Scan Test Logic



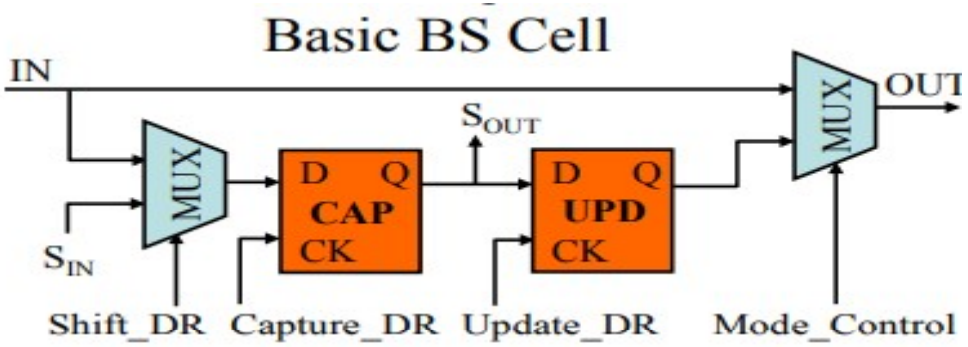
PC board test with boundary scan

FIGURE 10-13:
PC Board with Boundary Scan ICs



Link I/O cells of all ICs into one long scan chain

Boundary Scan Cell Architecture



BS Cell Operation

Operational Mode	Data Transfer
Normal	IN → OUT
Scan	S_{IN} → CAP
Capture	IN → CAP
Update	CAP → UPD

Boundary Scan Architecture

Additional logic :

- 1 Boundary Scan cell per I/O pin
- Test Access Port (TAP)
  - 4-wire interface
    - TMS
    - TCK
    - TDI
    - TDO
  - TAP controller
    - 16-state FSM
    - controlled by TMS & TCK
  - various registers for
    - instructions
    - operations