LAKIREDDY BALI REDDY COLLEGE OF ENGINEERING
(AUTONOMOUS)
Accredited by NAAC & NBA (CSE, IT, ECE, EEE & ME)
Approved by AICTE, New Delhi and Affiliated to JNTUK, Kakinada
L.B.Reddy Nagar, Mylavaram-521230, Krishna Dist, Andhra Pradesh, India

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE HANDOUT

PART-A

Name of Course Instructor : Mr. Sasi Bhushan K

Course Name & Code : Digitla VLSI System Design – 20VE01

L-T-P Structure : 3-0-0 Credits : 3

Program/Sem/Sec : M.Tech.- I-Sem & VLSI & ES A.Y : 2020-21

Pre-Requisites: Switching Theory & Logic Design, Computer organization.

Course Educational Objectives: In this course student will learn about the design of various combinational and sequential circuits using verilog HDL and VHDL, write the verilog tasks, functions and various digital modules

Course Outcomes (COs): At the end of the course, students are able to

CO 1	Design combinational and sequential circuits.
CO 2	Understand Digital System Design flow using verilog HDL
CO 3	Model Digital System Using Verilog HDL
CO 4	Write verilog Tasks, Functions, UDPs for Digital modules

Course Articulation Matrix (Correlation between COs &POs, PSOs):

COs	PSO1	PSO2	PSO3	PSO4	PSO5
CO1	1	--	--	--	3
CO2	--	3	2	3	--
CO3	--	2	2	3	--
CO4	--	--	--	3	--

Note: Enter Correlation Levels **1** or **2** or **3.** If there is no correlation, **put '-'**
1-Slight(Low), **2**-Moderate(Medium), **3**-Substantial (High).

TEXT BOOK(S):

T1 "Digital Systems Design using VERILOG" Charles H. Roth, Lizykurian John

Reference BOOK(S):

R1 Principles of CMOS VLSI Design – N.H.E. Weste, K. Eshraghian, 2nd Ed. Adisson Wesley.

R2 CMOS VLSI Design A Circuits and Systems perspective Third Edition, Neil H.E.Weste.

R3 Introduction to VLSI Systems – A Logic, Circuit and System Perspective – Ming Bo, Liu, CRC Press, 1st Edition, 2011

PART-B

COURSE DELIVERY PLAN (LESSON PLAN):

UNIT-I: Review of Logic Design Fundamentals

S.No.	Topic/s	No. of Classes Required	Tentative Date of Completion	Actual Date of Completion	Teaching Learning Methods	HOD Sign Weekly
1.	COs PSOs, Vision and Mission Department and Embedded systems overview, Combinational Logic, Boolean Algebra and Algebraic Simplification, Karnaugh Maps	1	22.02.2021			
2.	Designing with NAND and NOR Gates, Hazards in Combinational Circuits	1	23.02.2021			
3.	Flip-Flops and Latches, Mealy Sequential Circuit Design	1	24.02.2021			
4.	Design of a Moore Sequential Circuit	1	01.03.2021			
5.	Equivalent States and Reduction of State Tables	1	02.03.2021			
6.	Sequential Circuit Timing	1	03.03.2021			
7.	Tristate Logic and Busses	1	08.03.2021			
8.	Assignment/Tutorial / Seminar	1	09.03.2021			
No. of classes required to complete UNIT-I		**08**	No. of classes taken			

UNIT-II: Introduction to Verilog

S.No.	Topic/s	No. of Classes Required	Tentative Date of Completion	Actual Date of Completion	Teaching Learning Methods	HOD Sign Weekly
9.	Computer-Aided Design ,Hardware Description Languages, Verilog Description of Combinational Circuits	1	10.03.2021			
10.	Verilog Modules, Assignments, Procedural Assignments	1	15.03.2021			
11.	Modeling Flip-Flops Using Always Block , Always Blocks Using Event Control Statements	1	16.03.2021			
12.	Delays in Verilog, Compilation, Simulation, and Synthesis of Verilog Code	1	17.03.2021			
13.	Verilog Data Types and Operators, Simple Synthesis Examples	1	22.03.2021			
14.	Verilog Models for Multiplexers, Modeling Registers and Counters Using Verilog Always Statements	1	23.03.2021			
15.	Behavioral and Structural Verilog , Constants , Arrays	1	24.03.2021			
16.	Loops in Verilog, Testing a Verilog Model, A Few Things to Remember.	1	29.03.2021			
17.	Assignment/ Seminar	1	30.03.2021			
No. of classes required to complete UNIT-I		**09**	No. of classes taken			

UNIT-III: Design Examples

S.No.	Topic/s	No. of Classes Required	Tentative Date of Completion	Actual Date of Completion	Teaching Learning Methods	HOD Sign Weekly
18.	BCD to 7-Segment Display Decoder, A BCD Adder, 32-Bit Adders	1	12.04.2021			
19.	Traffic Light Controller , State Graphs for Control Circuits	1	13.04.2021			
20.	Scoreboard and Controller, Synchronization and Debouncing	1	19.04.2021			
21.	A Shift-and-Add Multiplier , Array Multiplier	1	20.04.2021			
22.	A Signed Integer/Fraction Multiplier	1	21.04.2021			
23.	Keypad Scanner, Binary Dividers	1	26.04.2021			
24.	Assignment / Tutorial / Seminar	1	27.04.2021			
No. of classes required to complete UNIT-III			**07**	No. of classes taken		

UNIT-IV: SM Charts and Microprogramming

S.No.	Topic/s	No. of Classes Required	Tentative Date of Completion	Actual Date of Completion	Teaching Learning Methods	HOD Sign Weekly
25.	State Machine Charts, Derivation of SM Charts , Realization of SM Charts	1	28.04.2021			
26.	Implementation of the Dice Game	1	03.05.2021			
27.	Microprogramming , Linked State Machines	1	04.05.2021			
28.	Assignment / Tutorial / Seminar	1	05.05.2021			
No. of classes required to complete UNIT-IV			**04**	No. of classes taken		

UNIT-V: Additional Topics in Verilog

S.No.	Topic/s	No. of Classes Required	Tentative Date of Completion	Actual Date of Completion	Teaching Learning Methods	HOD Sign Weekly
29.	Verilog Functions , Tasks , Multi-valued Logic and Signal Resolution, Built-in Primitives, User-Defined Primitives	1	10.05.2021			
30.	SRAM Model, Model for SRAM Read/Write System, Rise and Fall Delays of Gates	1	11.05.2021			
31.	Named Association, Generate Statements, System Functions	1	12.05.2021			
32.	Compiler Directives, File I/O Functions, Timing Checks	1	17.05.2021			
33.	The RISC Philosophy, The MIPS ISA, MIPS Instruction Encoding , Implementation of a MIPS Subset, Verilog Model	1	18.05.2021			
34.	Assignment / Tutorial / Seminar	1	19.05.2021			
No. of classes required to complete UNIT-V		**06**	No. of classes taken			

Teaching Learning Methods			
TLM1	Chalk and Talk	**TLM4**	Demonstration (Lab/Field Visit)
TLM2	PPT	**TLM5**	ICT (NPTEL/Swayam Prabha/MOOCS)
TLM3	Tutorial	**TLM6**	Group Discussion/Project

PART-C

EVALUATION PROCESS:

Evaluation Task	Marks
MID – I	M1 = 40
MID – II	M2 = 40
CIE Marks: A = 75% of Max(M1, M2) + 25% of Min(M1, A=M2)	M=40
Semester End Examinations (SEE)	S = 60
Total Marks = CIE + SEE	100

PART-D

PROGRAMME SPECIFIC OUTCOMES (PSOs):

PSO 1:	To independently carry out research/investigation and development work to solve practical problems.
PSO 2:	To write and present a substantial technical report/document
PSO 3:	To demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.
PSO4:	To Use different software tools in the domain of VLSI and Embedded Systems Design, Analysis and Verification such as Design entry, Synthesis, Functional and Timing Simulation, Floor planning, Place and route, Layout editors and RTL schematic.
PSO5:	To apply the appropriate design methodology to optimize various aspects for real-time processing in the field of VLSI and Embedded systems in favour of Industrial application

Date:

Course Instructor	Course Coordinator	Module Coordinator	HOD
Mr. Sasi Bhushan K	Mr. Sasi Bhushan K	Dr. P Lachi Reddy	Dr. Y. Amar Babu

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE HANDOUT

PART-A

Name of Course Instructor : Mr. M K Linga Murthy

Course Name & Code : Embedded System Design – 20VE02

L-T-P Structure : 3-0-0 Credits : 3

Program/Sem/Sec : M.Tech.- I-Sem & VLSI & ES A.Y : 2020-21

Pre-Requisites: Computer organization fundamentals, Microprocessors and microcontrollers fundamentals.

Course Objectives: This course provides the knowledge on typical embedded system components, characteristics and quality attributes of embedded systems, embedded hardware design and development, ARM architecture, IC Technology and Design technology to implement embedded system.

Course Outcomes (COs): At the end of the course, students are able to

CO 1	Choose different design methodologies to implement given specifications.
CO 2	Design control unit and Data path unit for given Embedded System.
CO 3	Use ARM processor architecture for development of Embedded System.
CO 4	Develop interface between ARM processor core, memory and co-processor.
CO5	Build frame work for embedded system using IC & design technology.

Course Articulation Matrix (Correlation between COs &POs, PSOs):

COs	PSO1	PSO2	PSO3	PSO4	PSO5
CO1	3	2	1	-	-
CO2	1	-	2	3	-
CO3	1	-	3	3	3
CO4	-	-	3	-	3

Note: Enter Correlation Levels **1** or **2** or **3.** If there is no correlation, **put '-'**
1-Slight(Low), **2**-Moderate(Medium), **3**-Substantial (High).

TEXT BOOK(S):

T1 "Embedded System Design A unified Hardware/Software Introduction" Frank Vahid/Tony Givargis, John Wiley & Sons Ptd

T2 "ARM System-on chip Architecture", 2nd edition,

PART-B

COURSE DELIVERY PLAN (LESSON PLAN):

UNIT-I: Discrete Embedded System Introduction

S.No.	Topic/s	No. of Classes Required	Tentative Date of Completion	Actual Date of Completion	Teaching Learning Methods	HOD Sign Weekly
1.	COs PSOs, Vision and Mission Department and Embedded systems overview, Design challenge	1	22.02.2021			
2.	Processor technology, IC technology	1	25.02.2021			
3.	Design Technology, Trade offs	1	26.02.2021			
4.	Single purpose processors	1	01.03.2021			
5.	RT-level combinational logic, Sequential logic	1	04.03.2021			
6.	RT-level-Custom single purpose processor design	1	05.03.2021			
7.	Optimizing custom single purpose processors	1	08.03.2021			
8.	Assignment	1	12.03.2021			
No. of classes required to complete UNIT-I		**08**	No. of classes taken			

UNIT-II: State Machine and Concurrent Process Models

S.No.	Topic/s	No. of Classes Required	Tentative Date of Completion	Actual Date of Completion	Teaching Learning Methods	HOD Sign Weekly
9.	State Machine and Concurrent Process Models – introduction, Models Vs Languages, Text Vs Graphics	1	15.03.2021			
10.	finite state machines with data path model (FSMD) – state machines	1	18.03.2021			
11.	program state machine model (PSM)	1	19.03.2021			
12.	concurrent process model , concurrent processes	1	22.03.2021			
13.	Communication among processes, Synchronization among processes	1	25.03.2021			
14.	Implementation	1	26.03.2021			
15.	Data flow model, Real time systems	1	01.04.2021			
16.	Assignment / Seminar	1	02.04.2021			
No. of classes required to complete UNIT-I		**08**	No. of classes taken			

UNIT-III: ARM Processor Architecture

S.No.	Topic/s	No. of Classes Required	Tentative Date of Completion	Actual Date of Completion	Teaching Learning Methods	HOD Sign Weekly
17.	ARM programmer's model	1	12.04.2021			
18.	ARM development tools	1	15.04.2021			
19.	ARM Assembly Language Programming	1	16.04.2021			
20.	Data processing instructions	1	19.04.2021			
21.	Data transfer instructions and Control flow instructions	1	22.04.2021			
22.	writing simple assembly language	1	23.04.2021			

	programs					
No. of classes required to complete UNIT-III			**06**	No. of classes taken		

UNIT-IV: ARM Organization and Implementation

S.No.	Topic/s	No. of Classes Required	Tentative Date of Completion	Actual Date of Completion	Teaching Learning Methods	HOD Sign Weekly
23.	Introduction, 3-stage and 5-stage pipeline ARM organization.	1	26.04.2021			
24.	ARM instruction execution, ARM implementation.	1	29.04.2021			
25.	ARM coprocessor interface, ARM memory interface	1	30.04.2021			
26.	ARM Instruction Set	1	03.05.2021			
27.	Thumb Instruction Set	1	06.05.2021			
28.	writing simple assembly language programs	1	07.05.2021			
No. of classes required to complete UNIT-IV			**06**	No. of classes taken		

UNIT-V: IC & Design Technology

S.No.	Topic/s	No. of Classes Required	Tentative Date of Completion	Actual Date of Completion	Teaching Learning Methods	HOD Sign Weekly
29.	Full custom IC Technology, Semi custom IC Technology	1	10.05.2021			
30.	PLD IC Technology	1	13.05.2021			
31.	Design Technology – Automation	1	17.05.2021			
32.	Design Technology – Synthesis	1	20.05.2021			
33.	Verification- hardware / software co simulation, Reuse – Intellectual property cores, Design Process Models	1	21.05.2021			
No. of classes required to complete UNIT-V		**05**	No. of classes taken			

Teaching Learning Methods			
TLM1	Chalk and Talk	**TLM4**	Demonstration (Lab/Field Visit)
TLM2	PPT	**TLM5**	ICT (NPTEL/Swayam Prabha/MOOCS)
TLM3	Tutorial	**TLM6**	Group Discussion/Project

PART-C

EVALUATION PROCESS:

Evaluation Task	**Marks**
MID – I	M1 = 40
MID – II	M2 = 40
CIE Marks: A = 75% of Max(M1, M2) + 25% of Min(M1, A=M2)	M=40
Semester End Examinations (SEE)	S = 60
Total Marks = CIE + SEE	100

PART-D

PROGRAMME SPECIFIC OUTCOMES (PSOs):

PSO 1:	To independently carry out research/investigation and development work to solve practical problems.
PSO 2:	To write and present a substantial technical report/document
PSO 3:	To demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.
PSO4:	To Use different software tools in the domain of VLSI and Embedded Systems Design, Analysis and Verification such as Design entry, Synthesis, Functional and Timing Simulation, Floor planning, Place and route, Layout editors and RTL schematic.
PSO5:	To apply the appropriate design methodology to optimize various aspects for real-time processing in the field of VLSI and Embedded systems in favour of Industrial application

Date:

Course Instructor	**Course Coordinator**	**Module Coordinator**	**HOD**
Mr. M K Linga Murthy	Mr. M K Linga Murthy	Dr. P Lachi Reddy	Dr. Y. Amar Babu

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE HANDOUT

PART-A

Name of Course Instructor : Mr. A. Uday Kumar

Course Name & Code : CRYPTOGRAPHY AND NETWORK SECURITY-20VE03

L-T-P Structure : 3-0-0 Credits : 3

Program/Sem/Sec : M.Tech.- I-Sem & VLSI & ES A.Y : 2020-21

PRE-REQUISITE: Computer Networks

COURSE EDUCATIONAL OBJECTIVES (CEOs): This course provides the knowledge on various security attacks and their characteristics, analyze the cryptographic techniques, concepts of digital signatures and its applications.

COURSE OUTCOMES (COs): At the end of the course, students are able to

CO 1	Discuss various types of attacks and their characteristics.
CO 2	Analyze various cryptographic techniques.
CO 3	Design public key cryptographic algorithms using the concepts from number theory.
CO 4	Describe the concept of digital signature and its applications.
CO5	Illustrate the concepts of IP and Web security.

COURSE ARTICULATION MATRIX (Correlation between COs, POs & PSOs):

COs	PSO1	PSO2	PSO3	PSO4	PSO5
CO1	1	-	2	-	3
CO2	2	2	3	-	3
CO3	-	2	3	-	3
CO4	-	2	3	-	3
CO5	1	-	-	-	2

Note: Enter Correlation Levels **1** or **2** or **3.** If there is no correlation, **put '-'**
1- Slight (Low), **2** – Moderate (Medium), **3** - Substantial (High).

BOS APPROVED TEXT BOOKS:

T1	"Cryptography and Network Security: Principles and Practice"- William Stallings, 2000, PE.

BOS APPROVED REFERENCE BOOKS:

R1	"Principles of Network and Systems Administration", Mark Burgess, Johnwiel.

PART-B

COURSE DELIVERY PLAN (LESSON PLAN):

UNIT-I: Introduction

S.No.	Topics to be covered	No. of Classes Required	Tentative Date of Completion	Actual Date of Completion	Teaching Learning Methods	Learning Outcome COs	Text Book followed	HOD Sign Weekly
1.	COs PSOs, Vision and Mission Department and Introduction	1	23.02.2021					
2.	Attacks , Service and Mechanisms	1	24.02.2021					
3.	Security Attacks and Security Services	1	26.02.2021					
4.	A Model for Internetwork Security	1	02.03.2021					
5.	Conventional Encryption Model	1	03.03.2021					
6.	Classical Encryption Techniques							
7.	Substitution Methods	1	05.03.2021					
8.	Transposition Methods							
9.	Playfair cipher							
10.	Stegnography							
11.	Overview of Unit 1	1	09.03.2021					
12.	Test -I							
13.	Assignment							
				No. of classes required to complete UNIT-I			**08**	
				No. of classes taken				

UNIT-II: Modern Techniques, Algorithms, Conventional Encryption, Public Key Cryptography.

S.No.	Topics to be covered	No. of Classes Required	Tentative Date of Completion	Actual Date of Completion	Teaching Learning Methods	Learning Outcome COs	Text Book followed	HOD Sign Weekly
14.	Introduction to Unit-II	1	10.03.2021					
15.	Simplified DES, Block Cipher Principles, Data Encryption Standard							
16.	Strength of DES, Differential and Linear Cryptanalysis, Block cipher design principles and modes.	1	12.03.2021					
17.	Triple DES, International Data Encryption Algorithm, Blowfish.	1	16.03.2021					
18.	RC5, CAST-128, RC2							
19.	Characteristics of Advanced Symmetric Block Ciphers	1	17.03.2021					
20.	Placement of Encryption function, Traffic Confidentiality	1	19.03.2021					
21.	Key Distribution							

22.	Random Number Generation	1	23.03.2021					
23.	RSA Algorithm							
24.	Key Management							
25.	Hiffie-Hellman key exchange, Elliptic key Cryptography	1	24.03.2021					
26.	Overview on Unit -II							
27.	Assignment							
No. of classes required to complete UNIT-II							**09**	
No. of classes taken								

UNIT-III: Number Theory, Message Authentication and Hash Functions.

S.No.	Topics to be covered	No. of Classes Required	Tentative Date of Completion	Actual Date of Completion	Teaching Learning Methods	Learning Outcome COs	Text Book followed	HOD Sign Weekly
28.	Introduction to Unit-III	1	26.03.2021					
29.	Prime and Relatively Prime Numbers							
30.	Modular Arithmetic, Fermats and Eulers Theorems	1	30.03.2021					
31.	Testing for primality, Euclid's Algorithm							
32.	The Chinese remainder theorem	1	31.03.2021					
33.	Discrete Logarithms	1	16.04.2021					
34.	Authentication requirements and functions							
35.	Message Authentication	1	20.04.2021					
36.	Hash Functions							
37.	Security of Hash Functions & MACs	1	23.04.2021					
38.	Assignment							
No. of classes required to complete UNIT-III							**06**	
No. of classes taken								

UNIT-IV : Hash and MAC Algorithms, Digital Signatures and Authentication protocols, Authentication Applications.

S.No.	Topics to be covered	No. of Classes Required	Tentative Date of Completion	Actual Date of Completion	Teaching Learning Methods	Learning Outcome COs	Text Book followed	HOD Sign Weekly
39.	Introduction	1	27.04.2021					
40.	MD File, Message Digest Algorithms							
41.	Secure Hash Algorithms, RIPEMD-160	1	28.04.2021					
42.	HMAC	1	30.04.2021					
43.	Digital Signatures, Authentication Protocols	1	04.05.2021					
44.	Digital signature standards							
45.	Kerberos, X.509, Directory Authentication Service	1	05.05.2021					
46.	Electronic Mail Security							

47.	Pretty Good Privacy, S/MIME	1	07.05.2021					
48.	Assignment							
No. of classes required to complete UNIT-IV							**06**	
No. of classes taken								

UNIT-V : IP Security, Web Security, Intruders, Viruses and Worms.

S.No.	Topics to be covered	No. of Classes Required	Tentative Date of Completion	Actual Date of Completion	Teaching Learning Methods	Learning Outcome COs	Text Book followed	HOD Sign Weekly
49.	Overview, Archiitecture	1	11.05.2021					
50.	Encapsulating Security Payload							
51.	Combining security Associations	1	12.05.2021					
52.	Key Management							
53.	Web Security Requirements, Secure Socket Layer	1	18.05.2021					
54.	Transport layer security, Secure Electronic Transaction							
55.	Intruders, viruses, Worms	1	19.05.2021					
56.	Viruses and related threats							
57.	Firewall Design Principles	1	21.05.2021					
58.	Trusted Systems							
59.	Assignment							
No. of classes required to complete UNIT-V							**05**	
No. of classes taken								

Contents beyond the Syllabus

S.No.	Topics to be covered	No. of Classes Required	Tentative Date of Completion	Actual Date of Completion	Teaching Learning Methods	HOD Sign Weekly
60.		1	02.01.2019			

Teaching Learning Methods			
TLM1	Chalk and Talk	**TLM4**	Demonstration (Lab/Field Visit)
TLM2	PPT	**TLM5**	ICT (NPTEL/Swayam Prabha/MOOCS/Moodle)
TLM3	Tutorial	**TLM6**	Group Discussion/Project

PART-C

EVALUATION PROCESS:

Evaluation Task	COs	Marks

MID – I	1, 2	40
MID – II	3, 4, 5	40
Evaluation of Mid Marks: A = 75% of Max(A1, A2) + 25% of Min(A1, A2)	1,2,3,4,5	**A=40**
Semester End Examinations	**1,2,3,4,5**	**B=60**
Total Marks: A+B	**1,2,3,4,5**	**100**

PART D

PROGRAMME SPECIFIC OUTCOMES (PSOs):

PSO 1:	To independently carry out research/investigation and development work to solve practical problems.
PSO 2:	To write and present a substantial technical report/document
PSO 3:	To demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.
PSO4:	To Use different software tools in the domain of VLSI and Embedded Systems Design, Analysis and Verification such as Design entry, Synthesis, Functional and Timing Simulation, Floor planning, Place and route, Layout editors and RTL schematic.
PSO5:	To apply the appropriate design methodology to optimize various aspects for real-time processing in the field of VLSI and Embedded systems in favour of Industrial application

Date:

Course Instructor	Course Coordinator	Module Coordinator	HOD
Mr. A. Uday Kumar	Mr. A. Uday Kumar	Dr.P. Lachi Reddy	Dr. Y. Amar Babu

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE HANDOUT

PART-A

Name of Course Instructor : Mrs. B.Rajeswari

Course Name & Code : Image and Video Processing & 20VE06

L-T-P Structure : 3-0-0 Credits : 3

Program/Sem/Sec : M.Tech.- I-Sem & VLSI & ES A.Y : 2020-21

PRE-REQUISITES : Digital Image Processing.

Course Objective**:** In this course student will learn about various compression, enhancement and segmentation techniques, image transformation techniques, and algorithms for 2D video signals.

Course Outcomes(COs): At the end of the course, student will be able to

CO 1	Examine different image transformation techniques.
CO 2	Evaluate various image enhancement and segmentation techniques.
CO 3	Analyze different compression techniques for images.
CO 4	Infer time-varying image formation models in video.
CO 5	Compare 2-D motion estimation algorithms for video signals.

Course Articulation Matrix (Correlation between COs &POs, PSOs):

Cos	PSO1	PSO2	PSO3	PSO4	PSO5
CO1	3	3	1	-	-
CO2	1	3	2	-	-
CO3	2	2	2	-	-
CO4	2	2	1	-	-
CO5	2	2	1	-	-

Note: Enter Correlation Levels **1** or **2** or **3.** If there is no correlation, **put '-'**

1- Slight(Low), **2 -** Moderate(Medium), **3 -** Substantial (High).

BOS APPROVED TEXT BOOKS:

1. Digital Image Processing – Gonzaleze and Woods, 3rd ed., Pearson.
2. Video processing and communication – Yao Wang, JoemOstermann and Ya–quin Zhang, 1st Ed., PH Int.

References :

Digital Video Processing – M. Tekalp, Prentice Hall International

PART B

COURSE DELIVERY PLAN (LESSON PLAN):

UNIT-I : Fundamentals of Image Processing and Image Transforms:

S.No.	Topics to be covered	No. of Classes Required	Tentative Date of Completion	Actual Date of Completion	Teaching Learning Methods	HOD Sign Weekly
1.	Introduction to Image processing, Fundamentals of image processing system,	1	22.02.2021			
2.	Applications of Digital image processing, Basic steps of Image Processing system	1	25.02.2021			
3.	Sampling and Quantization of an image	1	26.02.2021			
4.	Basic Relationship between pixels.	1	01.03.2021			
5.	Introduction to image transforms	1	04.03.2021			
6.	Fourier transform, 2 D Discrete Fourier transform	1	05.03.2021			
7.	Discrete Cosine Transform , Wavelet Transform ,CWT and DWT	1	08.03.2021			
No. of classes required to complete UNIT-I		07	No. of classes taken:			

UNIT-II : Image Processing Techniques : Image Enhancement, Image Segmentation

S.No.	Topics to be covered	No. of Classes Required	Tentative Date of Completion	Actual Date of Completion	Teaching Learning Methods	HOD Sign Weekly
8.	Introduction to Image processing Techniques, Basic Intensity transformation function	1	11.03.2021			
9.	Introduction to image enhancement, Enhancement in spatial domain	1	12.03.2021			
10.	Introduction to Histogram processing, Histogram manipulation	1	15.03.2021			
11.	Fundamentals of spatial filtering, Spatial filtering methods: Smoothing and Sharpening filters	1	18.03.2021			
12.	Introduction and Basics of filtering in frequency domain, Smoothing techniques, Selective filtering	1	19.03.2021			
13.	Sharpening filtering techniques	1	22.03.2021			

14.	Image Segmentation- Line, point, Edge detection	1	26.03.2021			
15.	Thresholding and its types,	1	29.03.2021			
No. of classes required to complete UNIT-II		08	No. of classes taken:			

UNIT-III : Image Compression

S.No.	Topics to be covered	No. of Classes Required	Tentative Date of Completion	Actual Date of Completion	Teaching Learning Methods	HOD Sign Weekly
16.	Introduction to Image compression, Image Compression Fundamentals	1	01.04.2021			
17.	Coding Redundancy, Spatial and Temporal redundancy	1	02.04.2021			
18.	Introduction to compression models, Lossy and Lossless compression	1	05.04.2021			
19.	Huffman coding, LZW Coding	1	12.04.2021			
20.	Run length coding, Biplane coding, JPEG Standards	1	16.04.2021			
21.	Huffman Coding, Arithmetic coding, Transform coding	1	19.04.2021			
22.	Wavelet coding, Predictive coding	1	22.04.2021			
No. of classes required to complete UNIT-III		07	No. of classes taken:			

UNIT-IV : Basic steps of Video Processing

S.No.	Topics to be covered	No. of Classes Required	Tentative Date of Completion	Actual Date of Completion	Teaching Learning Methods	HOD Sign Weekly
23.	Introduction to Video and its Processing, Basics steps of video Processing	1	23.04.2021			
24.	Analog video , Digital video	1	26.04.2021			
25.	Image formation and its models	1	29.04.2021			
26.	3-D Motion models, Geometric image formation	1	30.04.2021			
27.	Photometric Image formation, Filtering Operations.	1	03.05.2021			
28.	Sampling of analog and digital Video signals,	1	06.05.2021			

No. of classes required to complete UNIT-IV	06	No. of classes taken:

UNIT-V : 2-D Motion Estimation

S.No.	Topics to be covered	No. of Classes Required	Tentative Date of Completion	Actual Date of Completion	Teaching Learning Methods	HOD Sign Weekly
29.	Optical flow, General methodologies	1	10.05.2021			
30.	Pixel based motion estimation, Applications of motion estimation in video coding.	1	13.05.2021			
31.	Block Matching algorithm, Deformable block matching algorithms	1	14.05.2021			
32.	Mesh based Motion estimation, Global motion estimation	1	17.05.2021			
33.	Region based Motion estimation, Multi Resolution motion estimation	1	20.05.2021			
34.	Waveform based coding, Block based transform coding, Predictive coding	1	21.05.2021			
No. of classes required to complete UNIT-V		06	No. of classes taken:			

Teaching Learning Methods					
TLM1	Chalk and Talk	**TLM4**	Problem Solving	**TLM7**	Seminars or GD
TLM2	PPT	**TLM5**	Programming	**TLM8**	Lab Demo
TLM3	Tutorial	**TLM6**	Assignment or Quiz	**TLM9**	Case Study

PART C

ACADEMIC CALENDAR:

Description	From	To	Weeks
I Phase of Instructions	22.02.2021	10.04.2021	7W
I Mid Examinations	05.04.2021	10.04.2021	1W
II Phase of Instructions	12.04.2021	29.05.2021	7W
II Mid Examinations	24.05.2021	29.05.2021	1W
Preparation and Practicals	31.05.2021	05.06.2021	1W
Semester End Examinations	07.06.2021	19.06.2021	2W

EVALUATION PROCESS:

Evaluation Task	COs	Marks
I-Mid Examination	1,2	M1=40
II-Mid Examination	3,4,5	M2=40
Evaluation of Mid Marks: M=75% of Max(M1,M2)+25% of Min(M1,M2)	1,2,3,4,5	M=40
Semester End Examinations : S	**1,2,3,4,5**	**S=60**
Total Marks: CIE+SEE	**1,2,3,4,5**	**100**

PART-D

PROGRAMME SPECIFIC OUTCOMES (PSOs):

PSO 1:	To independently carry out research/investigation and development work to solve practical problems.
PSO 2:	To write and present a substantial technical report/document
PSO 3:	To demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.
PSO4:	To Use different software tools in the domain of VLSI and Embedded Systems Design, Analysis and Verification such as Design entry, Synthesis, Functional and Timing Simulation, Floor planning, Place and route, Layout editors and RTL schematic.
PSO5:	To apply the appropriate design methodology to optimize various aspects for real-time processing in the field of VLSI and Embedded systems in favour of Industrial application

B.Rajeswari	B.Rajeswari	Dr.G.L.N.Murthy	Dr.Y.Amar Babu
Course Instructor	**Course Coordinator**	**Module Coordinator**	**BOS Chairman&HOD**

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE HANDOUT
PART-A

Name of Course Instructor : Dr. Poornaiah Billa

Course Name & Code : RESEARCH METHODOLOGY and IPR & 20RM01

L-T-P Structure : 3-0-0 Credits : 3

Program/Sem/Sec : M.Tech.- I-Sem & VLSI & ES A.Y : 2020-21

Pre-Requisites: None

Course Objectives:

- To understand the research problem
- To know the literature studies, plagiarism and ethics
- To get the knowledge about technical writing
- To analyze the nature of intellectual property rights and new developments
- To know the patent rights

Course Outcomes (COs): At the end of the course, students are able to

CO 1	Understand research problem formulation and ethics
CO 2	Analyze research related information.
CO 3	Understand the process of patenting and development.
CO 4	Understand the importance of IPR in growth of individuals & nation.
CO5	Understand the necessity of IPR protection in R & D for creation of new products for economic growth and social benefits.

Course Articulation Matrix (Correlation between COs &POs, PSOs):

COS	PSO1	PSO2	PSO3	PSO4	PSO5
CO1	3	3	1	-	-
CO2	3	3	1	-	-
CO3	3	2	1	-	-
CO4	3	2	1	-	-
CO5	3	2	1		

Note: Enter Correlation Levels **1** or **2** or **3.** If there is no correlation, **put '-'**
1-Slight(Low), **2**-Moderate(Medium), **3**-Substantial (High).

TEXT BOOK(S):

T1 "Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students" Wayne Goddard and Stuart Melville,

T2 "Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction".

T3. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide for beginners".

REFERENCES

1. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.
2. Mayall, "Industrial Design", McGraw Hill, 1992.
3. Niebel, "Product Design", McGraw Hill, 1974.
4. Asimov, "Introduction to Design", Prentice Hall, 1962.
5. Robert P. Merges, Peter S. Menell, Mark A. Lemley, " Intellectual Property in New Technological Age", 2016.
6. T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand, 2008

PART-B

COURSE DELIVERY PLAN (LESSON PLAN):

UNIT I- RESEARCH PROBLEM AND SCOPE FOR SOLUTION

S.No.	Topic/s	No. of Classes Required	Tentative Date of Completion	Actual Date of Completion	Teaching Learning Methods	HOD Sign Weekly
35.	COs PSOs, Vision and Mission Department and Embedded systems overview, Design challenge	1	23.02.2021			
36.	Meaning of research problem, Sources of research problem	1	24.02.2021			
37.	Criteria Characteristics of a good research problem, Errors in selecting a research problem	1	25.02.2021			
38.	Scope and objectives of research problem	1	02.03.2021			
39.	Approaches of investigation of solutions for research problem	1	03.03.2021			
40.	data collection, analysis	1	04.03.2021			
41.	interpretation, Necessary instrumentations	1	09.03.2021			
42.	Assignment	1	10.03.2021			
No. of classes required to complete UNIT-I		**08**	No. of classes taken			

UNIT II- FORMAT

S.No.	Topic/s	No. of Classes Required	Tentative Date of Completion	Actual Date of Completion	Teaching Learning Methods	HOD Sign Weekly
43.	Effective literature studies approaches, analysis	1	11.03.2021			

44.	Plagiarism, Research ethics	1	16.03.2021			
45.	Effective technical writing, how to write report	1	17.03.2021			
46.	Paper Developing a Research Proposal	1	18.03.2021			
47.	Format of research proposal	1	23.03.2021			
48.	a presentation and assessment by a review committee	1	24.03.2021			
49.	Assignment / Seminar	1	25.03.2021			
No. of classes required to complete UNIT-I		**07**	No. of classes taken			

UNIT III- PROCESS AND DEVELOPMENT

S.No.	Topic/s	No. of Classes Required	Tentative Date of Completion	Actual Date of Completion	Teaching Learning Methods	HOD Sign Weekly
50.	Introduction to Nature of Intellectual Property	1	30.03.2021			
51.	Patents, Designs, Trade and Copyright	1	31.03.2021			
52.	Process of Patenting and Development	1	01.04.2021			
53.	technological research, innovation	1	13.04.2021			
54.	patenting, development	1	15.04.2021			
55.	International Scenario: International cooperation on Intellectual Property	1	20.04.2021			
56.	. Procedure for grants of patents, patenting under PCT	1	21.04.2021			
No. of classes required to complete UNIT-III :07				No. of classes taken		

UNIT IV- PATENT RIGHTS

S.No.	Topic/s	No. of Classes Required	Tentative Date of Completion	Actual Date of Completion	Teaching Learning Methods	HOD Sign Weekly
57.	Introduction to Patent Rights: Scope of Patent Rights	1	22.04.2021			
58.	Licensing and transfer of technology	1	27.04.2021			
59.	Patent information and databases. Geographical Indications	1	28.04.2021			
60.	Geographical Indications	1	29.04.2021			
61.	Review	1	04.05.2021			
No. of classes required to complete UNIT-IV: 05				No. of classes taken		

UNIT V- NEW DEVELOPMENTS IN IPR

S.No.	Topic/s	No. of Classes	Tentative Date of	Actual Date of	Teaching Learning	HOD Sign

		Required	Completion	Completion	Methods	Weekly
62.	New Developments in IPR: Administration of Patent System	1	05.05.2021			
63.	New developments in IPR; IPR of Biological Systems	1	06.05.2021			
64.	New developments in IPR - Computer Software etc	1	11.05.2021			
65.	Traditional knowledge Case Studies IPR and IITs	1	12.05.2021			
66.	Review		13.05.2021 to 28.05.2021			
No. of classes required to complete UNIT-V		**04**	No. of classes taken			

Teaching Learning Methods			
TLM1	Chalk and Talk	**TLM4**	Demonstration (Lab/Field Visit)
TLM2	PPT	**TLM5**	ICT (NPTEL/Swayam Prabha/MOOCS)
TLM3	Tutorial	**TLM6**	Group Discussion/Project

PART-C

EVALUATION PROCESS:

Evaluation Task	**Marks**
MID – I	M1 = 40
MID – II	M2 = 40
CIE Marks: A = 75% of Max(M1, M2) + 25% of Min(M1, A=M2)	M=20
Semester End Examinations (SEE)	S = 60
Total Marks = CIE + SEE	100

PART-D

PROGRAMME SPECIFIC OUTCOMES (PSOs):

PSO 1:	To independently carry out research/investigation and development work to solve practical problems.
PSO 2:	To write and present a substantial technical report/document
PSO 3:	To demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.
PSO4:	To Use different software tools in the domain of VLSI and Embedded Systems Design, Analysis and Verification such as Design entry, Synthesis, Functional and Timing Simulation, Floor planning, Place and route, Layout editors and RTL schematic.
PSO5:	To apply the appropriate design methodology to optimize various aspects for real-time processing in the field of VLSI and Embedded systems in favour of Industrial application

Date:

Course Instructor	**Course Coordinator**	**Module Coordinator**	**HOD**
Dr.Poornaiah Billa	Dr. Poornaiah Billa	Dr. P Lachi Reddy	Dr. Y. Amar Babu

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE HANDOUT

PART-A

Name of Course Instructor : Dr. M. Venkata Sudhakar

Course Name & Code : English for Research Paper Writing (ERPW)

L-T-P Structure : 2-0-0 Credits : 0

Program/Sem/Sec : M.Tech.- I-Sem & VLSI & ES A.Y : 2020-21

Course Objectives: This course gives knowledge on research paper writing skills. This course also describes the different section of the research paper. This course also provides skills that are needed for publication which includes paper preparation, plagiarism check and submission process.

Course Outcomes (COs): At the end of the course, students are able to

CO 1	Understand research article readability and writing skills.
CO 2	Identify essential parameters of each section of research articles.
CO 3	Apply the knowledge for writing and submit research paper for publication
CO 4	Develop skills that are required to maintain quality of research paper

Course Articulation Matrix (Correlation between COs &POs, PSOs):

COs	PSO1	PSO2	PSO3	PSO4	PSO5
CO1	2	2	-	-	-
CO2	1	2	-	-	-
CO3	1	1	-	-	-
CO4	1	2	-	-	-

Note: Enter Correlation Levels **1** or **2** or **3.** If there is no correlation, **put '-'**
1-Slight(Low), **2**-Moderate(Medium), **3**-Substantial (High).

TEXT BOOK(S):

T1 Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011

T2 Day, Robert A., How to Write and Publish a Scientific Paper, Cambridge University Press, 2006.

PART-B

COURSE DELIVERY PLAN (LESSON PLAN):

UNIT-I: Research paper Writing Skills Part-I

S.No.	Topic/s	No. of Classes Required	Tentative Date of Completion	Actual Date of Completion	Teaching Learning Methods	HOD Sign Weekly
1.	COs, PSOs, V and Overview of the course	1	22.02.2021			
2.	Planning and Preparation	1	25.02.2021			
3.	Word Order	1	26.02.2021			
4.	Breaking up long sentences	1	01.03.2021			
5.	Structuring	1	04.03.2021			
6.	Paragraphs and Sentences	1	05.03.2021			
7.	Being Concise	1	08.03.2021			
8.	Removing Redundancy	1	12.03.2021			
No. of classes required to complete UNIT-I		**08**	No. of classes taken			

UNIT-II: Research paper Writing Skills Part-II

S.No.	Topic/s	No. of Classes Required	Tentative Date of Completion	Actual Date of Completion	Teaching Learning Methods	HOD Sign Weekly
9.	Avoiding Ambiguity	1	15.03.2021			
10.	Vagueness	1	18.03.2021			
11.	Clarifying Who Did What	1	19.03.2021			
12.	Highlighting Your Findings	1	22.03.2021			
13.	Hedging	1	25.03.2021			
14.	Criticising	1	26.03.2021			
15.	Paraphrasing	1	01.04.2021			
16.	Plagiarism	1	02.04.2021			
No. of classes required to complete UNIT-I		**08**	No. of classes taken			

UNIT-III: Parts of research Paper

S.No.	Topic/s	No. of Classes Required	Tentative Date of Completion	Actual Date of Completion	Teaching Learning Methods	HOD Sign Weekly
17.	Title, Abstract	1	12.04.2021			
18.	Introduction,	1	15.04.2021			
19.	Review of the Literature	1	16.04.2021			
20.	Methods,	1	19.04.2021			
21.	Results, Discussion	1	22.04.2021			
22.	Conclusions, the Final Check.	1	23.04.2021			
No. of classes required to complete UNIT-III			**06**	No. of classes taken		

UNIT-IV: Preparation of manuscript

S.No.	Topic/s	No. of Classes Required	Tentative Date of Completion	Actual Date of Completion	Teaching Learning Methods	HOD Sign Weekly
23.	Key skills are needed when writing a Title, an Abstract	1	26.04.2021			

24.	An Introduction, , a Review of the Literature	1	29.04.2021			
25.	The Methods	1	30.04.2021			
26.	The Results, the Discussion,	1	03.05.2021			
27.	Conclusions	1	06.05.2021			
28.	Preparing the tables and figures	1	07.05.2021			
No. of classes required to complete UNIT-IV			**06**	No. of classes taken		

UNIT-V: Publishing the Paper

S.No.	Topic/s	No. of Classes Required	Tentative Date of Completion	Actual Date of Completion	Teaching Learning Methods	HOD Sign Weekly
29.	Rights and Permission,	1	10.05.2021			
30.	How to Submit the Manuscript,	1	13.05.2021			
31.	The Review Process	1	17.05.2021			
32.	The Publishing Process	1	20.05.2021			
33.	After Publication.	1	21.05.2021			
No. of classes required to complete UNIT-V		**05**	No. of classes taken			

Teaching Learning Methods			
TLM1	Chalk and Talk	**TLM4**	Demonstration (Lab/Field Visit)
TLM2	PPT	**TLM5**	ICT (NPTEL/Swayam Prabha/MOOCS)
TLM3	Tutorial	**TLM6**	Group Discussion/Project

PART-C

EVALUATION PROCESS:

Evaluation Task	Marks
CIE Marks:	100
Total Marks = CIE	100

PART-D

PROGRAMME SPECIFIC OUTCOMES (PSOs):

PSO 1:	To independently carry out research/investigation and development work to solve practical problems.
PSO 2:	To write and present a substantial technical report/document
PSO 3:	To demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.
PSO4:	To Use different software tools in the domain of VLSI and Embedded Systems Design, Analysis and Verification such as Design entry, Synthesis, Functional and Timing Simulation, Floor planning, Place and route, Layout editors and RTL schematic.
PSO5:	To apply the appropriate design methodology to optimize various aspects for real-time processing in the field of VLSI and Embedded systems in favour of Industrial application

Date:

Course Instructor	Course Coordinator	Module Coordinator	HOD
Dr. M Venkata Sudhakar	Dr. M Venkata Sudhakar	Dr. P Lachi Reddy	Dr. Y. Amar Babu

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE HANDOUT

PART-A

Name of Course Instructor : Mr. Sasi Bhushan K

Course Name & Code : Digital VLSI System Design Lab – 20VE60

L-T-P Structure : 0-0-2 Credits : 1

Program/Sem/Sec : M.Tech., ECE., VLSI & ES A.Y : 2020-21

Pre-Requisites:

Course Objectives: In This Laboratory student will learn about Modeling of CMOS logic circuits using Pyxis Schematic Editor, modeling of combinational and sequential logic circuits using VHDL/Verilog and implementation of digital circuits using FPGA.

Course Outcomes (COs): At the end of the course, students are able to

CO1	Design CMOS Logic gates using Pyxis Schematic Editor.
CO2	Model digital modules using VHDL/Verilog and Simulate.
CO3	Verify Implementation of Digital Design on FPGA Board.

Course Articulation Matrix (Correlation between COs &POs, PSOs):

COs	PSO 1	PSO 2	PSO 3	PSO 4	PSO 5
CO1	1	2	3	3	--
CO2	1	2	3	3	3
CO3	--	--	--	2	--
CO4	1	2	3	3	-

Note: Enter Correlation Levels **1** or **2** or **3.** If there is no correlation, **put '-'**
1-Slight(Low), **2**-Moderate(Medium), **3**-Substantial (High).

TEXT BOOK(S):

T1 JHON.F.Wakerly, "Digital Design Principles & Practices" III Edition, Prentice Hall Publishers.

Embedded System Design Lab (LESSON PLAN):

Expt. No	Experiment/s	No. of Classes Required	Tentative Date of Completion	Actual Date of Completion	Teaching Learning Methods	HOD Sign Weekly
CYCLE-1						
1	Design of 8 input priority encoder and 3 to 8 Decoder	3	24.02.2021		**TLM5,8**	
2	Design of 8x1Mux and 1x8 Demux	3	03.03.2021		**TLM5,8**	
3	Design of 4 bit adder	3	10.03.2021		**TLM5,8**	
4	Design 4 bit Magnitude Comparator	3	17.03.2021		**TLM5,8**	
5	Design of BCD adder	3	24.03.2021		**TLM5,8**	
6	Design of ALU	3	31.03.2021		**TLM5,8**	
7	Design of D,T,JK Flip Flops	3	21.04.2021		**TLM5,8**	
8	Design of Shift Registers	3	28.04.2021		**TLM5,8**	
CYCLE-2						
9	Design of Counters	3	05.05.2021		**TLM5,8**	
10	Design of FSM(Moore's Machine)	3	12.05.2021		**TLM5,8**	
11	Design of FSM(Mealy Machine)		12.05.2021		**TLM5,8**	
12	Design CMOS Inverter	3	19.05.2021		**TLM5,8**	
13	Design NAND gate		19.05.2021		**TLM5,8**	
14	Internal Exam	3	20.05.2021		--	

Teaching Learning Methods			
TLM1	Chalk and Talk	**TLM4**	Demonstration (Lab/Field Visit)
TLM2	PPT	**TLM5**	ICT (NPTEL/Swayam Prabha/MOOCS)
TLM3	Tutorial	**TLM6**	Group Discussion/Project

EVALUATION PROCESS:

Evaluation Task	**Marks**
Day to Day work	A1 = 20
Viva – Voce during Lab Sessions	A2 = 10
Internal Lab Examination	A3 = 10
Cumulative Internal Examination : A1+A2+A3	**40**
Semester End Examinations : C	**60**
Total Marks: A1+A2+A3+C	**100**

Date:

Mr. Sasi Bhushan K	Mr. Sasi Bhushan K	Dr. P Lachi Reddy	Dr. Y Amar Babu
Course Instructor	**Course Coordinator**	**Module Coordinator**	**HOD**

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE HANDOUT

PART-A

Name of Course Instructor : Mr. M K Linga Murthy

Course Name & Code : Embedded System Design Lab – 20VE61

L-T-P Structure : 0-0-2 Credits : 1

Program/Sem/Sec : M.Tech., ECE., VLSI & ES A.Y : 2020-21

Pre-Requisites: Microprocessors and Microcontrollers Fundamentals.

Course Objectives: In This Course student will learn about the programming in Assembly language programs on ARM processor kits, programming on CPLD and FPGA kits using EDK tools.

Course Outcomes (COs): At the end of the course, students are able to

CO1	Develop the Assembly Language Programs for ARM processors.
CO2	Develop the interfacing programs for ARM processors and I/O devices.
CO3	Design an Embedded System using the FPGA and EDK tools.

Course Articulation Matrix (Correlation between COs &POs, PSOs):

COs	PSO 1	PSO 2	PSO 3	PSO 4	PSO 5
CO1	**1**	**2**	**3**	**3**	**-**
CO2	**1**	**2**	**3**	**3**	**-**
CO3	**1**	**2**	**3**	**3**	**3**
CO4	**1**	**2**	**3**	**3**	**-**

Note: Enter Correlation Levels **1** or **2** or **3.** If there is no correlation, **put '-'**
1-Slight(Low), **2**-Moderate(Medium), **3**-Substantial (High).

TEXT BOOK(S):

T1 "ARM System-on chip Architecture", 2nd edition, Steve Ferber, Addison wesley

Embedded System Design Lab (LESSON PLAN):

Expt. No	Experiment/s	No. of Classes Required	Tentative Date of Completion	Actual Date of Completion	Teaching Learning Methods	HOD Sign Weekly
1	Introduction Lab experiments	3	23.02.2021		TLM2	
2	ARM Assembly Language Programming-I ARM Assembly Language Programming-II	3	02.03.2021		TLM 2,4	
3	Program to Interface 8 Bit LED Program to demonstrate Time delay program using built in Timer / Counter feature	3	09.03.2021		TLM 2,4	
4	Program to Displaying a message in a 2 line x 16 Characters LCD display and verify the result in debug terminal	3	16.03.2021		TLM 2,4	
5	Generation of PWM Signal	3	23.03.2021		TLM 2,4	
6	. Serial Communication	3	30.03.2021		TLM 2,4	
7	Traffic light Controller	3	20.04.2021		TLM 2,4	
8	Stepper motor Controller	3	27.04.2021		TLM 2,4	
9	Program to demonstrate I2C Interface on IDE environment	3	04.05.2021		TLM 5,8	
10	Design of System On Chip platform using Xilinx FPGAs and Embedded Development Kit Hardware Software co-design using Xilinx EDK Tools and advanced FPGS Board Zynq 7000 series	3	11.05.2021		TLM 2,4	
11	Internal Lab Examination	3	18.05.2021		--	

Teaching Learning Methods			
TLM1	Chalk and Talk	**TLM4**	Demonstration (Lab/Field Visit)
TLM2	PPT	**TLM5**	ICT (NPTEL/Swayam Prabha/MOOCS)
TLM3	Tutorial	**TLM6**	Group Discussion/Project

EVALUATION PROCESS:

Evaluation Task	**Marks**
Day to Day work	A1 = 20
Viva – Voce during Lab Sessions	A2 = 10
Internal Lab Examination	A3 = 10
Cumulative Internal Examination : A1+A2+A3	**40**
Semester End Examinations : C	**60**
Total Marks: A1+A2+A3+C	**100**

Mr. M K Linga Murthy	Mr. M K Linga Murthy	Dr. P Lachi Reddy	Dr. Y Amar Babu
Course Instructor	**Course Coordinator**	**Module Coordinator**	**HOD**