M. Tech. (VLSI System Design)
PG Course Structure-R25

I-SEMESTER

S. No	Course Code	Course Title	Contact hours/week			Credits	Scheme of Valuation		
			L	T	P		CIE	SEE	Total
THEORY COURSES									
1	D2516101	Digital CMOS Circuit Design	3	1	0	4	40	60	100
2	D2516102	Analog CMOS Circuit Design	3	1	0	4	40	60	100
3	D2516103	MOS Device Physics	3	1	0	4	40	60	100
4	**PROGRAM ELECTIVE – I**		3	0	0	3	40	60	100
5	**PROGRAM ELECTIVE – II**		3	0	0	3	40	60	100
LABORATORY COURSES									
6	D2516190	Digital CMOS Circuit Design Lab	0	1	2	2	40	60	100
7	D2516191	Analog CMOS Circuit Design Lab	0	1	2	2	40	60	100
8	D2516180	Seminar – I	0	0	2	1	100	--	100
Total			**15**	**5**	**6**	**23**	**380**	**420**	**800**

List of Professional Elective Courses in I Semester (Electives – I & II)

S. No.	Course Code	Course Title
1	D25161A0	VLSI Technology
2	D25161A1	Nano Scale Devices
3	D25161A2	MOS Devices Modelling and Characterization
4	D25161A3	Digital System Design through HDL
5	D25161B0	VLSI Architectures
6	D25161B1	Power Management IC Design
7	D25161B2	Low Power Design Techniques
8	D25161B3	CAD for VLSI

@ Minimum 2/3 themes per elective

II-SEMESTER

S. No	Course Code	Course Title	Contact hours/week			Credits	Scheme of Valuation		
			L	T	P		CIE	SEE	Total
THEORY COURSES									
1	D2526101	CMOS Mixed Signal Circuit Design	3	1	0	4	40	60	100
2	D2526102	Physical Design Verification	3	1	0	4	40	60	100
3	D2526103	VLSI Testing & Testability	3	1	0	4	40	60	100
4	**PROGRAM ELECTIVE – III**		3	0	0	3	40	60	100
5	**PROGRAM ELECTIVE – IV**		3	0	0	3	40	60	100
LABORATORY COURSES									
6	D2526190	CMOS Mixed Signal Circuit Design Lab	0	1	2	2	40	60	100
7	D2526191	Physical Design Verification Lab	0	1	2	2	40	60	100
8	D2526180	Seminar – II	0	0	2	1	100	--	100
Total			**15**	**5**	**6**	**23**	**380**	**420**	**800**

List of Professional Elective Courses in II Semester (Electives III & IV)

S. No.	Course Code	Course Title
1	D25261A0	VLSI signal processing
2	D25261A1	MEMS & NEMS
3	D25261A2	SoC design
4	D25261A3	Fundamentals of Semiconductor Package Manufacturing and Test
5	D25261B0	Advanced VLSI Interconnects
6	D25261B1	Quantum Computing
7	D25261B2	RF IC Design
8	D25261B3	NANO ELECTRONICS

@ Minimum 2/3 themes per elective

III-SEMESTER

S. No	Course Code	Course Title	Contact hours/week			Credits	Scheme of Valuation		
			L	T	P		CIE	SEE	Total
THEORY COURSES									
1	D2536101/M	Research Methodology and IPR / Swayam 12-Weeks MOOC Course – RM & IPR	3	0	0	3	40	60	100
LABORATORY COURSES									
2	D253610S	Summer Internship/Industrial Training (8-10 Weeks)*	-	-	-	3	100	-	100
3	D25361CV	Comprehensive Viva#	-	-	-	2	100	-	100
4	D253610P	Dissertation Part-A$	-	-	20	10	100	-	100
Total			**3**	**0**	**20**	**18**	**340**	**60**	**400**

*** Student attended during summer/year break and assessment will be done in 3rd Semester.**
 # Comprehensive Viva can be conducted courses completed up to 2nd Semester.
$ Dissertation Part-A: Internal Assessment.

IV-SEMESTER

S. No	Course Code	Course Title	Contact hours/week			Credits	Scheme of Valuation		
			L	T	P		CIE	SEE	Total
1	D254610P	Dissertation Part-B%	-	-	32	16	-	100	100
Total			**-**	**-**	**32**	**16**	**-**	**100**	**100**

% External Assessment

M. Tech. (VLSI System Design)
I-Semester
Detailed Syllabus

D2516101 – Digital CMOS Circuit Design

M. Tech. (I-Sem.)

L	T	P	Cr.
3	1	0	4

Course Outcomes (COs): At the end of the course, students will be able to

CO1: Analyze MOSFET behavior and CMOS inverter characteristics under static and dynamic conditions. **(Analyze-L4)**
CO2: Design various combinational and sequential logic blocks using CMOS technology. **(Apply-L3)**
CO3: Optimize data path elements such as adders, multipliers, and barrel shifters. **(Apply-L3)**
CO4: Design and evaluate memory architectures including SRAM and ROM cells. **(Apply-L3)**
CO5: Interpret and implement circuit layouts using stick diagrams and layout rules. **(Apply-L3)**

UNIT-I:

MOS Transistor Principles and CMOS Inverter:
MOSFET characteristics under Static and Dynamic Conditions, MOS Transistor Secondary Effects, CMOS Inverter – Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay Parameters, Stick Diagram and Layout Diagrams.

UNIT-II:

Combinational Logic Circuits: Static CMOS Design, Different Styles of Logic Circuits, Logical Effort of Complex Gates, Static and Dynamic Properties of Complex Gates, Interconnect Delay, Dynamic Logic Gates.

UNIT-III:

Sequential Logic Circuits: Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines, Non-Bistable Sequential Circuits.

UNIT-IV:

Arithmetic Building Blocks: Data Path Circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs.

UNIT-V:

Memory Architectures: Memory Architectures and Memory Control Circuits: Read-Only Memories, ROM Cells, Read-Write Memories (RAM), Dynamic Memory Design, 6-Transistor SRAM Cell, Sense Amplifiers.

TEXT BOOKS:

1. JanRabaey, Anantha Chandrakasan, B Nikolic, "Digital Integrated Circuits: A Design Perspective", Prentice Hall of India, 2nd Edition, Feb 2003
2. N. Weste, K. Eshraghian,"Principles of CMOS VLSI Design", Addision Wesley, 2nd Edition, 1993.

REFERENCE BOOKS:

1. MJ Smith, "Application Specific Integrated Circuits", AddissonWesley,1997
2. Sung-Mo Kang &Yusuf Leblebici, "CMOS Digital Integrated Circuits Analysis and Design", McGraw-Hill,1998

D2516102 – Analog CMOS Circuit Design

M. Tech. (I-Sem.)

L	T	P	Cr.
3	1	0	4

Course Outcomes (COs): At the end of the course, students will be able to

CO1: Design basic building blocks of CMOS Analog ICs. **(Apply-L3)**
CO2: Carry out the design of single and two stage operational amplifiers and voltage references. **(Apply-L3)**
CO3: Determine the device dimensions of each MOSFETs involved. **(Apply-L3)**
CO4: Design various amplifiers like differential, current and operational amplifiers. **(Apply-L3)**

UNIT-I:

MOS Devices and Modeling: The MOS Transistor, Passive Components - Capacitor & Resistor, Integrated Circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT-II:

Analog CMOS Sub-Circuits: MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors - Current Mirror with Beta Helper, Degeneration, Cascode Current Mirror and Wilson Current Mirror, Current and Voltage References, Bandgap Reference.

UNIT-III:

Single Stage Amplifier: Common Source Stage with Resistive Load, Diode Connected Load, Triode Load, CS Stage with Source Degeneration, Source Follower, CG Stage, Gain Boosting Techniques, Cascode, Folded Cascode, Choice of Device Models.

UNIT-IV:

CMOS Amplifiers and Noise: Inverters, Differential Amplifiers, Cascode Amplifiers. Noise - Statistical Characteristics, Types, Noise in Single- Stage Amplifiers, Noise in Differential Pairs, Noise Bandwidth.

UNIT-V:

CMOS Operational Amplifiers: Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of Op Amps.

TEXT BOOKS:

1. CMOS Analog Circuit Design -Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.

REFERENCE BOOKS:

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R.G. Meyer, Wiley India, Fifth Edition, 2010.
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI

D2516103 – MOS Device Physics

M. Tech. (I-Sem.)

L	T	P	Cr.
3	1	0	4

Course Outcomes (COs): At the end of the course, students will be able to

CO1: Understand the electrostatics and energy band behavior of MOS structures. **(Understand-L2)**
CO2: Analyze and model MOSFETs using classical and advanced physical principles. **(Analyze-L4)**
CO3: Evaluate SOI-based MOSFET devices and their operational characteristics. **(Evaluate-L5)**
CO4: Apply quantum and ballistic transport concepts to nanoscale transistor design. **(Apply-L3)**
CO5: Explore and assess modern MOSFET structures including FinFETs and Strained-Si devices **(Analyze-L4)**

UNIT-I:

MOS Capacitor: Energy Band Diagram of Metal-Oxide-Semiconductor Contacts, Modes of Operation – Accumulation, Depletion, Midgap, and Inversion, 1D Electrostatics of MOS, Depletion Approximation, Accurate Solution of Poisson's Equation, CV Characteristics of MOS, LFCV and HFCV, Non-Idealities in MOS – Oxide Fixed Charges, Interfacial Charges, Midgap Gate Electrode, Poly-Silicon Contact, Electrostatics of Non-Uniform Substrate Doping, Ultrathin Gate-Oxide and Inversion Layer Quantization, Quantum Capacitance, MOS Parameter Extraction.

UNIT-II:

Physics of MOSFET: Drift-Diffusion Approach for I–V Characteristics, Gradual Channel Approximation, Sub-threshold Current and Slope, Body Effect, Pao & Sah Model, Detailed 2D Effects in MOSFET, High Field and Doping Dependent Mobility Models, High Field Effects and MOSFET Reliability Issues (SILC, TDDB, and NBTI), Leakage Mechanisms in Thin Gate Oxide, High-K Metal Gate MOSFET Devices and Technology Issues, Intrinsic MOSFET Capacitances and Resistances, Meyer Model.

UNIT-III:

SOI MOSFET: FDSOI and PDSOI, 1D Electrostatics of FDSOI MOS, VT Definitions, Back Gate Coupling and Body Effect Parameter, I–V Characteristics of FDSOI-FET, FDSOI Sub-Threshold Slope, Floating Body Effect, Single Transistor Latch, ZRAM Device, Bulk and SOI FET – Discussions Referring to the ITRS.

UNIT-IV:

Nanoscale Transistors: Diffusive, Quasi-Ballistic, and Ballistic Transports, Ballistic Planar and Nanowire FET Modeling – Semi- Classical and Quantum Treatments.

UNIT-V:

Advanced MOSFETs: Strain Engineered Channel Materials, Mobility in Strained Materials, Electrostatics of Double Gate and FinFET Devices.

TEXT BOOKS:

1. S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, Wiley.
2. Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press.
3. M. Lundstrom and J. Guo, *Nanoscale Transistors: Device Physics, Modeling& Simulation*, Springer

REFERENCE BOOKS:

1. Y. Tsividis, *Operation and Modeling of the MOS Transistor*, Oxford University Press.
2. J. P. Colinge, *Silicon-on-Insulator Technology: Materials to VLSI*, Springer.
3. Selected research papers in relevant and emerging areas

M. Tech. (I-Sem.)

D25161A0–VLSI Technology
(PE – I)

L	T	P	Cr.
3	0	0	3

Course Outcomes (COs): At the end of the course, students will be able to

CO1: To understand the semiconductor materials, devices and technology historical evaluation. **(Understand-L2)**
CO2: To analyze the oxidization process and quality measures in the fabrication. **(Analyze-L4)**
CO3: To explain lithography importance in the semiconductor industry and the various Techniques. **(Understand-L2)**
CO4: To apply other process steps like etching, implantation and metallization and their applications. **(Apply-L3)**
CO5: To understand the concepts of electrical testing and packaging of ICs. **(Understand-L2)**

UNIT-I:
Introduction: Semiconductor materials, semiconductor devices, semiconductor process technology, basic fabrication steps. Crystal Growth: Silicon crystal growth from melt, silicon float-zone process, GaAs crystal growth techniques, material characterization.

UNIT-II:
Silicon Oxidation: Thermal oxidation, impurity redistribution during oxidation, masking of silicon dioxide, oxide quality. Photolithography: Optical lithography, E-beam lithography.

UNIT-III:
Etching: Wet chemical etching, dry etching. Diffusion: Basic diffusion process, extrinsic diffusion, lateral diffusion.

UNIT-IV:
Ion Implantation: Range of implanted ions, implant damage and annealing. Film Deposition: Epitaxial growth techniques, structures and defects in epitaxial layers, dielectric deposition.

UNIT-V:
Process Integration: Passive components, bipolar technology, MESFET technology, MEMS technology. IC Manufacturing: Electrical testing, packaging.

TEXT BOOK:

1. Gary S May & Simon M Sze, Fundamentals of Semiconductor Fabrication, Wiley Student edition, 2012.

REFERENCE BOOKS:

1. S. K. Ghandhi, VLSI Fabrication Principles, John Wiley Inc, 2010.
2. S. M. Sze, VLSI Technology, 2/e, McGraw Hill, 2011.
3. Stephen Cambell, The Science and Engineering of Microelectronic Fabrication, Oxford University Press, 2013

M. Tech. (I-Sem.)

D25161A1 – Nano Scale Devices
(PE – I)

L	T	P	Cr.
3	0	0	3

Course Outcomes (COs): At the end of the course, students will be able to

CO1: Describe the physical behavior and scaling trends of long-channel and short-channel MOSFETs. **(Understand-L2)**
CO2: Understand short-channel effects and propose design solutions using advanced materials. **(Understand-L2)**
CO3: Analyze 3D transistor structures like FinFETs, DG-ETSOI, and nanowires. **(Analyze-L4)**
CO4: Apply concepts of ballistic and quasi-ballistic transport to nanoscale transistors. **(Analyze-L4)**
CO5: Explore ongoing trends such as NEGF and quantum dots for future Nanoelectronics. **(Apply-L3)**

UNIT-I:
Long Channel MOSFETs: History, Introduction – MOSFET as a Barrier-Controlled Device, MOSFET I–V Characteristics, Drain Current Models, MOSFET Scaling, Subthreshold Characteristics, Substrate Bias and Temperature Dependence, MOSFET Electrostatics – Energy Band Picture, 1D Electrostatic Poisson–Boltzmann Equation, Depletion Approximation, Onset of Inversion, Gate Voltage and Surface Potential, Static and Mobile Charges.

UNIT-II:
Short Channel Effects: Charge Sharing, Channel Length Modulation, DIBL, GIDL, Velocity Saturation, MOSFET Breakdown, Concepts of High-K/Metal Gate.

UNIT-III:
Advanced Planar and 3D Transistors: FDSOI, DG-ETSOI, FinFETs, Nanowires.

UNIT-IV:
Nanoscale Transport: Bottom-Up Approach, Landauer's Formalism, Ballistic and Diffusive Transport – Modes, I–V Characteristics, Conductance, Voltage Drop and Heat Dissipation, Ballistic MOSFET, Ballistic Injection Velocity, Virtual Source Model.

UNIT-V:
Current Topics and Open Issues: Strained Silicon Technology, NEGF, Thermoelectric Effects and Thermoelectric Devices, Quantum Dot Devices – Quantum Capacitance, I–V Characteristics, Self-Consistent Method.

TEXT BOOKS:

1. M. Lundstrom, *Fundamentals of Nanotransistors*, World Scientific.
2. T. H. Ning and Y. Taur, *Fundamentals of Modern VLSI Devices*, Pearson Education India Pvt. Ltd.

REFERENCE BOOKS:

1. D. A. Neamen, *Semiconductor Physics and Devices*, McGraw-Hill Higher Education.
2. S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, Wiley

M. Tech. (I-Sem.)

D25161A2 – MOS Devices Modeling and Characterization

(PE – I)

L	T	P	Cr.
3	0	0	3

Course Outcomes (COs): At the end of the course, students will be able to

CO1: Understand and derive the electrostatic and CV behavior of MOS capacitors. **(Understand-L2)**
CO2: Analyze threshold voltage variations and bias effects in MOS devices. **(Analuze-L4)**
CO3: Evaluate MOSFET operation across different regions and environmental conditions. **(Apply-L3)**
CO4: Apply small-signal models including Ebers-Moll and charge control for AC analysis. **(Apply-L3)**
CO5: Study and model short-channel effects in modern deep-submicron devices. **(Understand-L2)**

UNIT-I:

Basic Concepts: Energy Band Diagram of Metal-Oxide-Semiconductor Contacts, Modes of Operation – Accumulation, Depletion, Midgap, and Inversion, 1D Electrostatics of MOS, Depletion Approximation, Accurate Solution of Poisson's Equation.

UNIT-II:

Bias Conditions: CV Characteristics of MOS, LFCV and HFCV, Non- Idealities in MOS – Oxide Fixed Charges, Interfacial Charges, Threshold Voltage Capacitance-Voltage Relation, The Three-Terminal MOS Structure, Effect of Body Bias on Surface Conditions, Threshold Voltage with Body Bias.

UNIT-III:

MOSFETs: The Four-Terminal Metal-Oxide-Semiconductor Transistor, Strong Inversion, Moderate Inversion and Weak Inversion Current, Voltage Models, Effective Mobility, Effect of Source and Drain Series Resistance, Temperature Effects, Breakdown.

UNIT-IV:

Small Signal Models: Ebers-Moll Model, Charge Control Model, Small-Signal Models for Low and High Frequency, Switching Characteristics.

UNIT-V:

Short Channel Effects: Short Channel and Thin Oxide Effects, Carrier Velocity Saturation, Channel Length Modulation, Charge Sharing, Drain Induced Barrier Lowering (DIBL), Punch Through, Hot Carrier Effects, Impact Ionization, Velocity Overshoot, Ballistic Operation, Quantum Mechanical Effects, DC Gate Current, Junction Leakage, Band-to-Band Tunneling, Gate Induced Drain Leakage (GIDL), MOSFET Scaling.

TEXT BOOKS:

1. S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed., Wiley Eastern, 1981.
2. Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, 2013.

REFERENCE BOOKS:

1. Y. Tsividis and C. McAndrew, *The MOS Transistor*, 3rd ed., Oxford University Press, 2013.
2. Y. P. Tsividis, *Operation and Modelling of the MOS Transistor*, McGraw-Hill, 1987.
3. E. Takeda, *Hot-Carrier Effects in MOS Transistors*, Academic Press, 1995.

M. Tech. (I-Sem.)

D25161A3 – Digital System Design Through HDL
(PE – I)

L	T	P	Cr.
3	0	0	3

Course Outcomes (COs): At the end of the course, students will be able to

CO1: Design and simulate digital systems using VHDL and Verilog in behavioral, dataflow, and structural styles. **(Apply-L3)**
CO2: Implement combinational and sequential logic components in HDL. **(Apply-L3)**
CO3: Translate logic circuits into synthesizable HDL code using FSMs and control logic. **(Apply-L3)**
CO4: Use synthesis tools and interpret synthesized netlists for implementation. **(Apply-L3)**
CO5: Evaluate and test digital systems for faults using CAD tools and test methodologies. **(Apply-L3)**

UNIT-I:
Digital Logic Design using VHDL: Introduction, designing with VHDL, design entry methods, logic synthesis, entities, architecture, packages and configurations, types of models: dataflow, behavioral, structural, signals vs. variables, generics, data types, concurrent vs. sequential statements, loops and program controls. Digital Logic Design using Verilog HDL: Introduction, Verilog data types and operators, binary data manipulation, combinational and sequential logic design, structural models of combinational logic, logic simulation, design verification and test methodology, propagation delay, truth table models using Verilog.

UNIT-II:
Combinational Logic Circuit Design using VHDL: Combinational circuits building blocks: multiplexers, decoders, encoders, code converters, arithmetic comparison circuits, VHDL for combinational circuits, adders - half adder, full adder, ripple-carry adder, carry look- ahead adder, subtraction, multiplication. Sequential Logic Circuit Design using VHDL: Flip-flops, registers & counters, synchronous sequential circuits: basic design steps, Mealy state model, design of FSM using CAD tools, serial adder example, state minimization, design of counter using sequential circuit approach.

UNIT-III:
Digital Logic Circuit Design Examples using Verilog HDL: Behavioral modeling, data types, Boolean-equation-based behavioral models of combinational logics, propagation delay and continuous assignments, latches and level-sensitive circuits in Verilog, cyclic behavioral models of flip-flops and latches and edge detection, comparison of styles for behavioral model; behavioral model, multiplexers, encoders and decoders, counters, shift registers, register files, dataflow models of a linear feedback shift register, machines with multi cycle operations, ASM and ASMD charts for behavioral modeling, design examples, keypad scanner and encoder.

UNIT-IV:
Synthesis of Digital Logic Circuit Design: Introduction to synthesis, synthesis of combinational logic, synthesis of sequential logic with latches and flip-flops, synthesis of explicit and implicit state machines, registers and counters.

UNIT-V:
Testing of Digital Logic Circuits and CAD Tools: Testing of logic circuits, fault model, complexity of a test set, path-sensitization, circuits with tree structure, random tests, testing of sequential circuits, built-in self-test, printed circuit boards, computer aided design tools, synthesis, physical design.

TEXT BOOKS:

1. Stephen Brown & Zvonko Vranesic, "Fundamentals of Digital logic design with VHDL", Tata McGraw Hill,2nd edition.
2. Michael D. Ciletti, "Advanced digital design with the Verilog HDL", Eastern economy edition, PHI.

REFERENCE BOOKS:

1. Stephen Brown & Zvonko Vranesic, "Fundamentals of Digital logic with Verilog design", Tata McGraw Hill,2nd edition.
2. Bhaskar, "VHDL Primer",3rd Edition, PHI Publications.
3. Ian Grout, "Digital systems design with FPGAs and CPLDs", Elsevier Publications

M. Tech. (I-Sem.)

D25161B0 – VLSI Architectures
(PE – II)

L	T	P	Cr.
3	0	0	3

Course Outcomes (COs): At the end of the course, students will be able to
CO1: Design RISC architecture and control units for a given instruction set. **(Apply-L3)**
CO2: Improve the performance of RISC processors by applying pipelining techniques. **(Apply-L3)**
CO3: Translate DSP algorithms into efficient hardware architectures and design associated building blocks. **(Apply-L3)**
CO4: Analyze the impact of retiming, unfolding, and folding on the performance of DSP architectures. **(Analyze-L4)**

UNIT-I:
Instruction Set Architectures and CPU Performance: Overview of Instruction Set Architectures – CISC, RISC, and DSP Processors, CPU Performance and Its Factors, Evaluating Performance Metrics.

UNIT-II:
Design of RISC Processor: Designing the Datapath and Control Unit for a RISC Processor, Multicycle Implementation of RISC Architecture.

UNIT-III:
Enhancing Performance with Pipelining: Overview of Pipelining, Pipelined Datapath, Pipelined Control Unit, Pipeline Hazards – Data, Control, and Structural Hazards, Techniques for Hazard-Free Pipelined RISC Implementation.

UNIT-IV:
Multiprocessors and DSP Algorithm Representation: Introduction to Multiprocessors, Multiprocessors Connected by a Single Bus and Network, Network Topologies, Evolution vs. Revolution in Computer Architecture, DSP Algorithm Representation – Data Flow Graphs, Loop Bound and Iteration Bound, Algorithms for Computing Iteration Bound.

UNIT-V:
Pipelining, Parallel Processing, and VLSI Performance Techniques: Introduction to Pipelining and Parallel Processing, FIR Filter Pipelining, Parallel Processing Techniques, Pipelining and Parallel Processing for Low Power, VLSI Architecture Optimization Techniques – Retiming, Unfolding, and Folding.

TEXT BOOKS:

1. D.A,Patterson And J.L.Hennessy, Computer Organization and Design: Hardware/ Software Interface, Elsevier, 2011, 4th Edition
2. Keshab Parhi, VLSI digital signal processing systems design and Implementations, Wiley 1999
3. NPTEL Courses (https://nptel.ac.in/courses/108105157)

M. Tech. (I-Sem.)

D25161B1 – Power Management IC Design
(PE – II)

L	T	P	Cr.
3	0	0	3

Course Outcomes (COs): At the end of the course, students will be able to

CO1: Understand the need for power management circuits in modern VLSI systems. **(Understand-L2)**
CO2: Identify and explain various components of a power management system, with emphasis on DC-DC converters. **(Apply-L3)**
CO3: Design chip-level DC-DC converters based on given system-level specifications. **(Apply-L3)**
CO4: Apply a top-down design methodology to implement efficient DC-DC converter topologies. **(Apply-L3)**

UNIT-I:

Introduction to Power Management and Voltage Regulation: Introduction to power management and voltage regulators, need of power management, power management applications, classification of power management, power delivery of a VLSI system, power conversion, discrete vs. integrated power management, types of voltage regulators (switching vs. linear regulators) and applications, converter's performance parameters (voltage accuracy, power conversion efficiency, load regulation, line regulation, line and load transient response, settling time, voltage tracking), local vs. remote feedback, Kelvin sensing, Point-of-Load (POL) regulators.

UNIT-II:

Principles of Linear Voltage Regulators: Linear regulators, Low Drop- Out Regulator (LDO), source and sink regulators, shunt regulator, pass transistor, error amplifier, small signal and stability analysis, compensation techniques, current limiting, power supply rejection ratio (PSRR), NMOS vs. PMOS regulator, current regulator.

UNIT-III:

Switching DC-DC Converters: Design and Control Technique: Switching DC-DC converters and control techniques, types (buck, boost, buck-boost), power FETs, choosing L and C, PWM modulation (leading, trailing and dual edge modulation), losses in switching converters, output ripple, voltage vs. current mode control, CCM and DCM modes, small signal model of DC-DC converter, loop gain analysis of uncompensated DC-DC converter, type-I, type-II and type- III compensation, compensation of voltage mode and current mode DC- DC converters, hysteretic control, switched capacitor DC-DC converters

UNIT-IV:

Systematic Design of DC-DC Converters: Top-down design approach of a DC-DC converter, selecting topology, switching frequency and external components, sizing power FETs, segmented power FET, designing gate driver, PWM modulator, error amplifier, oscillator, ramp generator, feedback resistors, current sensing, PFM/PSM mode for light load, effect of parasitic on reliability and performance, current limit and short circuit protection, soft start control, chip level layout and placement guidelines, board level layout guidelines, EMI considerations.

UNIT-V:

Emerging Technologies in Power Management: Introduction to advanced topics in power management, digitally controlled DC-DC converters, digitally controlled LDOs, adaptive compensation, dynamic voltage scaling (DVS), Single-Inductor Multiple-Outputs (SIMO) converters, DC-DC converters for LED lighting, Li-ion battery charging circuits.

TEXT BOOKS:

1. Switch-mode Power Supplies: SPICE Simulations and Practical Designs, Christophe P Basso, BPB Publications, 2010.
2. Power Management Techniques for Integrated Circuit Design By Ke-Horng Chen,Wiley-Blackwell, 2016.

REFERENCE BOOKS:

1. Fundamentals of Power Electronics, 2nd edition by Robert W. Erickson, Dragan Maksimovic, Springer (India) Pvt. Ltd, 2005.
2. Bernhard Wicht, Design of Power Management Integrate Circuits, Wiley, 2024

M. Tech. (I-Sem.)

D25161B2 – Low Power Design Techniques
(PE – II)

L	T	P	Cr.
3	0	0	3

Course Outcomes (COs): At the end of the course, students will be able to

CO1: Understand the sources of power dissipation in CMOS circuits and estimation techniques. **(Understand-L2)**
CO2: Apply probabilistic and circuit-level techniques for low-power logic design. **(Apply-L3)**
CO3: Design power-efficient architectures using switching activity reduction and voltage scaling. **(Apply-L3)**
CO4: Analyze and reduce power consumption in clock distribution networks. **(Analyze-L4)**
CO5: Apply algorithmic and architectural techniques for system-level power optimization. **(Apply-L3)**

UNIT-I:
Introduction to Low Power Design: Need for low power VLSI chips, sources of power dissipation, device and technology impact on low power, impact of technology scaling, technology and device innovation, power estimation, SPICE circuit simulators, gate-level logic simulation, capacitive power estimation, static power, gate-level capacitance estimation, architecture-level analysis, Monte-Carlo simulation.

UNIT-II:
Probabilistic Power Analysis and Circuit-Level, Logic-Level Design: Random logic signals, probability and frequency, probabilistic power analysis techniques, signal entropy, low power design, power consumption in circuits, flip-flop and latch design, high capacitance nodes, low power digital cell libraries, gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic.

UNIT-III:
Low Power Architecture and Systems: Power and performance management, switching activity reduction, parallel architectures with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.

UNIT-IV:
Low Power Clock Distribution: Power dissipation in clock distribution, single driver vs. distributed buffers, zero skew vs. tolerable skew, chip and package co-design techniques for clock networks.

UNIT-V:
Algorithm and Architectural Level Methodologies: Introduction, design flow, algorithmic level analysis and optimization, architectural level estimation and synthesis.

TEXT BOOKS:

1. K. Roy and S. Prasad, *Low-Power CMOS VLSI Circuit Design*, Wiley, 2000.
2. G. K. Yeap, *Practical Low Power Digital VLSI Design*, Kluwer Academic Publishers (KAP), 2002.
3. J. M. Rabaey and M. Pedram (Eds.), *Low Power Design Methodologies*, Kluwer Academic Publishers, 1997.

M. Tech. (I-Sem.)

D25161B3 – CAD for VLSI
(PE – II)

L	T	P	Cr.
3	0	0	3

Course Outcomes (COs): At the end of the course, students will be able to
CO1: Understand the VLSI design flow and the stages of physical design automation. **(Understand-L2)**
CO2: Apply algorithms for partitioning, floor planning, pin assignment, and placement. **(Apply-L3)**
CO3: Analyze and implement routing algorithms for global and detailed routing. **(Analyze-L4)**
CO4: Explore physical design techniques for FPGAs and MCMs. **(Apply-L3)**
CO5: Design robust I/O circuits and understand ESD, latch-up prevention, and clock distribution challenges. **(Apply-L3)**

UNIT-I:
VLSI Physical Design Automation: VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles, System Packaging Styles.

UNIT-II:
Partitioning, Floor Planning, Pin Assignment and Placement: Partitioning – Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm, Simulated Annealing. Floor Planning – Problem formulation, Classification of floor planning algorithms, constraint-based floor planning, Rectangular Dualization. Pin Assignment – Problem formulation, Classification of pin assignment algorithms, General and channel pin assignments. Placement – Problem formulation, Classification of placement algorithms, Partitioning based placement algorithms.

UNIT-III:
Global Routing and Detailed Routing: Global Routing – Problem formulation, Classification of global routing algorithms, Maze routing algorithms. Detailed Routing – Problem formulation, Classification of routing algorithms, Single layer routing algorithms.

UNIT-IV:
Physical Design Automation of FPGAs and MCMs: FPGA Technologies, Physical Design cycle for FPGAs, Partitioning, Routing – Routing Algorithm for the Non-Segmented model, Routing Algorithms for the Segmented Model. Introduction to MCM Technologies, MCM Physical Design Cycle.

UNIT-V:
Chip Input and Output Circuits: ESD Protection, Input Circuits, Output Circuits and L(di/dt) noise, On-chip clock Generation and Distribution, Latch-up and its prevention.

TEXT BOOKS:
1. Algorithms for VLSI Physical Design Automation by Naveed Shervani, 3rd Edition, 2005, Springer International Edition.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:
1. VLSI Physical Design Automation-Theory and Practice by Sadiq M Sait, Habib Youssef, World Scientific.
2. Algorithms for VLSI Design Automation, S. H. Gerez, 1999, Wiley student Edition, John Wiley and Sons (Asia) Pvt. Ltd.
3. VLSI Physical Design Automation by Sung Kyu Lim, Springer International Edition.

D2516190 – Digital CMOS Circuit Design Lab

M. Tech. (I-Sem.)

L	T	P	Cr.
0	1	2	2

Course Outcomes (COs): At the end of the course, students will be able to
CO1: Have the ability to explain the VLSI Design Methodologies using Mentor Graphics Tools. **(Apply-L3)**
CO2: Grasp the significance of various design logic Circuits in full-custom IC Design. **(Apply-L3)**
CO3: Have the ability to explain the Physical Verification in Layout Extraction. **(Apply-L3)**
CO4: Fully Appreciate the design and analyze of CMOS Digital Circuits. **(Apply-L3)**
CO5: Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation. **(Apply-L3)**

List of Experiments:

1. Inverter Characteristics.
2. NAND and NOR Gate
3. XOR and XNOR Gate
4. 2:1 Multiplexer
5. Full Adder
6. RS-Latch
7. Clock Divider
8. JK-Flip Flop
9. Synchronous Counter
10. Asynchronous Counter
11. Static RAM Cell
12. Dynamic Logic Circuits
13. Linear Feedback Shift Register.

Lab Requirements:

Software:
Industry Standard Software (Mentor Graphics Tool/Cadence/ Synopsys/Equivalent)

Hardware:
Personal Computer with necessary peripherals, configuration and operating System

D2516191 – Analog CMOS Circuit Design Lab

M. Tech. (I-Sem.)

L	T	P	Cr.
0	1	2	2

Course Outcomes (COs): At the end of the course, students will be able to

CO1: Have the ability to explain the VLSI Design Methodologies using Mentor Graphics Tools. **(Apply-L3)**
CO2: Grasp the significance of various cmos analog circuits in full-custom IC Design flow. **(Apply-L3)**
CO3: Have the ability to explain the Physical Verification in Layout Design. **(Apply-L3)**
CO4: Fully Appreciate the design and analyze of analog and mixed signal simulation. **(Apply-L3)**
CO5: Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation. **(Apply-L3)**

List of Experiments:

1. MOS Device Characterization and parametric analysis
2. Common Source Amplifier
3. Common Source Amplifier with source degeneration
4. Cascode amplifier
5. Simple current mirror
6. Cascode current mirror.
7. Wilson current mirror.
8. Differential Amplifier
9. Operational Amplifier
10. Sample and Hold Circuit
11. Direct-conversion ADC
12. R-2R Ladder Type DAC.

Lab Requirements:

Software:
Mentor Graphics – Pyxis Schematic, IC Station, Calibre, ELDO Simulator/ Industry Equivalent Standard Software

Hardware:
Personal Computer with necessary peripherals, configuration and operating System.