# M.Tech (VLSI and Embedded Systems Design)

## R23-PG Course Structure

### I SEMESTER

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<tr>
<th>S. No</th>
<th>Course code</th>
<th>Course Title</th>
<th>Contact hours/week</th>
<th>Credits</th>
<th>Scheme of Valuation</th>
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<tr>
<td>1</td>
<td>23VE01</td>
<td>Digital VLSI System Design</td>
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<td>23VE03</td>
<td>Cryptography and Network Security</td>
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<td>23VE05</td>
<td>High speed VLSI Design</td>
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<td>Image and Video Processing</td>
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<td>23VE07</td>
<td>System Modeling and Simulation</td>
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<td>VLSI Design Automation</td>
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Total Credits: 18 + 18 + 16 + 16 = 68

#### List of Courses offered under Audit Course

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<th>Name of the Course</th>
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<tr>
<td>1</td>
<td>23AC01</td>
<td>English for Research Paper Writing</td>
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<td>2</td>
<td>23AC02</td>
<td>Disaster Management</td>
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<td>Sanskrit for Technical Knowledge</td>
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<td>23AC05</td>
<td>Constitution of India</td>
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<td>23AC06</td>
<td>Pedagogy Methods</td>
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<td>Stress Management by Yoga</td>
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<td>23AC08</td>
<td>Personality Development through Life Enlightenment Skills</td>
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#### List of Open Elective Courses offered to other Departments

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<tr>
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<tr>
<td>1</td>
<td>23VE81</td>
<td>CAD for VLSI Design</td>
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<td>23VE82</td>
<td>Programmable Logic Devices</td>
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<td>23VE83</td>
<td>VLSI Testing</td>
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</table>
M. Tech (VLSI & Embedded Systems)
I – Semester Detailed Syllabus
**Pre-Requisites:** STLD, CO

**COURSE EDUCATIONAL OBJECTIVES:**
In this course student will learn about the design of various combinational and sequential circuits using verilog HDL and VHDL, write the verilog tasks, functions, and various digital modules.

**COURSE OUTCOMES:** At the end of this course student will be able to
CO1: Design Combinational and Sequential circuits.
CO2: Understand Digital System Design flow using Verilog HDL.
CO3: Model Digital System Using Verilog HDL.
CO4: Write Verilog Tasks, Functions, UDPs for Digital modules.

**UNIT-I: REVIEW OF LOGIC DESIGN FUNDAMENTALS**

**UNIT-II: INTRODUCTION TO VERILOG**

**UNIT-III: DESIGN EXAMPLES**

**UNIT-IV: SM CHARTS AND MICROPORGRAMMING**

**UNIT-V: ADDITIONAL TOPICS IN VERILOG & DESIGN OF A RISC MICROPROCESSOR**

TEXT BOOK:

REFERENCE:
M. Tech. (I Sem.) 23VE02 – EMBEDDED SYSTEM DESIGN

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**Pre-Requisites:** Computer Organization, Microprocessors and Microcontrollers

**COURSE EDUCATIONAL OBJECTIVES:**
In this course student will learn about the design methodologies of embedded systems, design the control unit and data-path unit for a given embedded system, interface between ARM processor, memory and co-processor etc.

**COURSE OUTCOMES:** At the end of this course student will be able to
CO1: Choose different design methodologies to implement given specifications.
CO2: Design control unit and Data path unit for given Embedded System.
CO3: Use ARM processor architecture for development of Embedded System.
CO4: Develop interface between ARM processor core, memory and co-processor.
CO5: Build framework for embedded system using IC & design technology.

**Unit I: Embedded System Introduction:** Embedded systems overview, design challenge, processor technology, IC technology, Design Technology, Trade-offs. Single purpose processors RT-level combinational logic, sequential logic(RT level), custom single purpose processor design (RT –level), optimizing custom single purpose processors.

**Unit II: State Machine and Concurrent Process Models:** Introduction, models Vs languages, finite state machines with data path model(FSMD), using state machines, program state machine model (PSM), concurrent process model, concurrent process model, concurrent processes, communication among processes, synchronization among processes, Implementation, data flow model, real-time systems.

**Unit III: ARM Processor Architecture:** The ARM programmer's model, ARM development tools, ARM Assembly Language Programming: Data processing instructions, Data transfer instructions, Control flow instructions, writing simple assembly language programs.

**Unit IV: ARM Organization and Implementation:** 3-stage pipeline ARM organization, 5-stage pipeline ARM organization, ARM instruction execution, ARM implementation, The ARM coprocessor interface, The ARM memory interface, The ARM Instruction Set.

**Unit V: IC and Design Technology:** IC Technology: Full-Custom (VLSI) IC Technology, Semicustom(ASIC) IC Technology, Programmable logic device(PLD) IC technology, Design technology: automation: synthesis, verification: Hardware/Software Co-Simulation, Reuse: Intellectual Property cores, Design Process Models

**TEXT BOOKS:**
REFERENCES:

Pre-Requisites: Computer Networks

COURSE EDUCATIONAL OBJECTIVES:
In this course student will learn about the various security attacks and their characteristics, analyze the cryptographic techniques, concepts of digital signatures and its applications.

COURSE OUTCOMES: At the end of this course student will be able to
CO1: Discuss various types of attacks and their characteristics.
CO2: Analyze various cryptographic techniques.
CO3: Design public key cryptographic algorithms using the concepts from number theory.
CO4: Describe the concept of digital signature and its applications.
CO5: Illustrate the concepts of IP and Web security.

UNIT-I

UNIT-II
Block Ciphers and the Data Encryption Standard: Block Cipher Principles, Classical Feistel Network, Data Encryption Standard (DES) and DES Encryption, Strength of DES, Block Cipher Design Principles, Block Cipher Modes of operation: ECB, CBC, CFB, OFB, CTR, Blowfish Algorithm, Random Number Generation.

UNIT-III
Number theory: Prime and Relatively prime numbers, Modular arithmetic, Fermat’s and Euler’s theorems, Testing for primality, Euclid’s Algorithm, the Chinese remainder theorem, Discrete logarithms.

UNIT-IV
Hash and Mac Algorithms: MD File, Message digest Algorithm, Secure Hash Algorithm, RIPEMD-160, and HMAC.
UNIT-V
Intruders, Viruses and Worms: Intruders, Viruses and Related threats.
Fire Walls: Fire wall Design Principles, Trusted systems.

Text Book:

References:
1. Principles of Network and Systems Administration, Mark Burgess, John Wiely
Pre-Requisites: Networking Knowledge

COURSE EDUCATIONAL OBJECTIVES:
In this course student will learn about the Technologies used in IoT, build platform for various IoTs, analyzing the IoT architecture, performance and security aspects.

COURSE OUTCOMES: At the end of this course student will be able to
CO1: Understand technologies involved in IoT Development.
CO3: Analyze IoT architecture for performance and security aspects.
CO4: Develop IoT application using various protocols.
CO5: Integrate Big Data and Visualization issues in IoT.

UNIT I:
The IoT Networking Core : Technologies involved in IoT Development: Internet/Web and Networking Basics OSI Model, Data transfer referred with OSI Model, IP Addressing, Point to Point Data transfer, Point to Multi Point Data transfer & Network Topologies, Sub-netting, Network Topologies referred with Web, Introduction to Web Servers, Introduction to Cloud Computing

UNIT II:

UNIT III:

UNIT IV:

UNIT V:
TEXT BOOKS:
1. LoWPAN: The Wireless Embedded Internet, Zach Shelby, Carsten Bormann, Wiley
2. Internet of Things: Converging Technologies for Smart Environments and Integrated Ecosystems, Dr. OvidiuVermesan, Dr. Peter Friess, River Publishers
3. Interconnecting Smart Objects with IP: The Next Internet, Jean-Philippe Vasseur, Adam Dunkels, Morgan Kuffmann

REFERENCES:
1. The Internet of Things: From RFID to the Next-Generation Pervasive Networked Lu Yan, Yan Zhang, Laurence T. Yang, Huansheng Ning
2. Internet of Things (A Hands-on-Approach), Vijay Madisetti, Arshdeep Bahga
3. Designing the Internet of Things, Adrian McEwen (Author), Hakim Cassimally
Program Elective - I

M. Tech. (I Sem.)

23VE05 – HIGH SPEED VLSI DESIGN

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Pre-Requisites: VLSI Design

COURSE EDUCATIONAL OBJECTIVES:
In this course student will learn about the frequency and time metrics, various power and clock distribution techniques for ICs, and various Latching strategies used in ICs.

COURSE OUTCOMES: At the end of this course student will be able to

CO1: Analyze need for High speed VLSI design using frequency, time metrics.
CO2: Use power distribution on-chip for high speed chips.
CO3: Design signaling convention and circuits for on-chip transmission lines.
CO4: Resolve timing convention and synchronization issues on-chip.
CO5: Develop clocked, non clocked logic and latching strategies for high speed design.

UNIT I:
Introduction to high speed digital design: Frequency, time and distance issues in digital VLSI design. Capacitance and inductance effects, high speed properties of logic gates, speed and power. Modeling of wires, geometry and electrical properties of wires, Electrical models of wires, transmission lines, lossless LC transmission lines, lossy RLC transmission lines and special transmission lines.

UNIT II:

UNIT III:
Signaling convention and circuits: Signaling modes for transmission lines, signaling over lumped transmission media, signaling over RC interconnect, driving lossy LC lines, simultaneous bi-directional signaling terminations, transmitter and receiver circuits.

UNIT IV:
Timing convention and synchronization: Timing fundamentals, timing properties of clocked storage elements, signals and events, open loop timing, level sensitive clocking, pipeline timing, closed loop timing, clock distribution, synchronization failure and meta-stability, clock distribution, clock skew and methods to reduce clock skew, controlling crosstalk in clock lines, delay adjustments, clock oscillators and clock jitter - PLL and DLL based clock aligners.

UNIT V:
Clocked & non clocked Logics:
Single-Rail Domino Logic, Dual-Rail Domino Structures, Latched Domino Structures, Clocked Pass Gate Logic, Static CMOS, DCVS Logic, Non-Clocked Pass Gate Families.
Latching Strategies:
Basic Latch Design, and Latching single-ended logic and Differential Logic, Race Free Latches for Pre-charged Logic Asynchronous Latch Techniques.
TEXT BOOKS:

REFERENCE BOOKS:
Pre-Requisites: Digital Image Processing

COURSE EDUCATIONAL OBJECTIVES:
In this course student will learn about the various compression, enhancement and segmentation techniques, image transformation techniques, and algorithms for 2D video signals.

COURSE OUTCOMES: At the end of this course student will be able to
CO1: Examine different image transformation techniques.
CO2: Evaluate various image enhancement and segmentation techniques.
CO3: Analyze different compression techniques for images.
CO4: Infer time-varying image formation models in video.
CO5: Compare 2-D motion estimation algorithms for video signals.

UNIT I
Fundamentals of Image Processing and Image Transforms: Basic steps of Image Processing System Sampling and Quantization of an image – Basic relationship between pixels
Image Transforms: 2 D- Discrete Fourier Transform, Discrete Cosine Transform (DCT), Introduction to Wavelet Transforms.

UNIT II
Image Processing Techniques:
Image Segmentation: Segmentation concepts, Point, Line and Edge Detection, Thresholding, Region Based segmentation.

UNIT III
Image Compression: Image compression fundamentals - Coding Redundancy, Spatial and Temporal redundancy, Compression models: Lossy & Lossless, Huffman coding, Arithmetic coding, LZW coding, Run length coding, Bit plane coding, Transform coding, Predictive coding, Wavelet coding, JPEG Standards.

UNIT IV

UNIT V 2-D
Motion Estimation: Optical flow, General Methodologies, Pixel Based Motion Estimation, Block- Matching Algorithm, and Mesh based Motion Estimation, Global Motion Estimation, Region based Motion Estimation, Multi resolution motion estimation, Application of motion estimation in Video coding.
Text Books:

Reference:
Pre-Requisites: Random variables

COURSE EDUCATIONAL OBJECTIVES:
In this course student will learn about the various Simulation and Programming Models, Optimization methodologies.

COURSE OUTCOMES: At the end of this course student will be able to
CO1: Understand basic simulation models, characterizing and simulation diagrams.
CO2: Model time driven systems and stochastic processes.
CO3: Know how to simulate any discrete systems using queuing systems.
CO4: Discuss system optimization, modeling and simulation methodology.
CO5: Build simulation models with programming languages.

Unit – I

Unit – II

Unit – III

Unit – IV
System Optimization: System Identification, Searches, Alpha / Beta trackers, Multidimensional Optimization, Modeling and Simulation Methodology.

Unit – V
Simulation Software and Building Simulation Models:
Comparison of Simulation Packages with Programming Languages, Classification of Simulation Software, Desirable software features, General Purpose Simulation Packages-Arena, Extend; Guide lines for determining the level of Model detail, Techniques for increasing Model Viability and credibility.
TEXT BOOKS:

REFERENCES:
1. Systems Simulation - Geoffrey Gordan, PHI
Pre-Requisites: VLSI Design

COURSE EDUCATIONAL OBJECTIVES:
In this course student will learn about the design cycles, various techniques on Partitioning, Placement and Routing and addressing their problems.

COURSE OUTCOMES: At the end of this course student will be able to
CO1: Understand need for VLSI physical design automation.
CO2: Analyze VLSI automation algorithms for partitioning.
CO3: Formulate placement, floor planning and pin assignment problems and simulate.
CO4: Resolve routing issues using various algorithms.
CO5: Illustrate physical design cycle for FPGAs.

UNIT I:
VLSI Physical Design Automation: Introduction, VLSI Design cycle, new trends in VLSI design cycle, new trends in Physical design cycle, Design styles, full custom Basic terminology, complex issues, basic algorithms, Basic data structures, and algorithms.

UNIT II:

UNIT III:
Placement, Floor Planning & Pin Assignment: problem formulation, simulation base placement algorithms, other placement algorithms, constraint based floor planning, floor planning algorithms for mixed block & cell design. General & channel pin assignment

UNIT IV:
Global Routing: Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches
Detailed Routing: Problem formulation, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms.
Over The Cell Routing & Via Minimization: two layers over the cell routers, constrained & unconstrained via minimization

UNIT V:
Physical design Automation of FPGAs:
Introduction, FPGA Technologies, Physical design cycle for FPGAs, Partitioning, Routing, Routing algorithms for the non-segmented model, Routing algorithms for segmented model, routing algorithms for staggered model.

TEXT BOOK:
REFERENCE BOOKS:

Pre-Requisites: Knowledge in Engineering, English

COURSE EDUCATIONAL OBJECTIVES:
To understand the research problem, to know the literature studies, plagiarism and ethics, to get the knowledge about technical writing, to analyse the nature of intellectual property rights and new developments and research related information and to know the patent rights.

COURSE OUTCOMES: At the end of this course student will be able to
CO1: Analyze the research problem and its formulation.
CO2: Analyze the significance of research ethics.
CO3: Apply the information technology for better tomorrow and to develop creativity.
CO4: Identify the importance of intellectual property rights to be promoted among students in general and Engineering in particular.
CO5: Describe the IPR protection for new and better products, and in turn brings about, economic growth and social benefits.

UNIT I - RESEARCH PROBLEM AND SCOPE FOR SOLUTION

UNIT II - FORMAT
Effective literature studies approaches, analysis, Plagiarism, Research ethics. Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee.

UNIT III- PROCESS AND DEVELOPMENT

UNIT IV- PATENT RIGHTS

UNIT V- NEW DEVELOPMENTS IN IPR
New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.
TEXT BOOKS:
2. Wayne Goddard and Stuart Melville, “Research Methodology: An Introduction”

REFERENCES:
Pre-Requisites: Knowledge in English

Course Educational Objective:
This course gives knowledge on research paper writing skills. This course also describes the different sections of the research paper. This course also provides skills that are needed for publication which includes paper preparation, plagiarism check and submission process.

Course Outcomes (COs): At the end of the course, students will be able to
CO1: Understand research article readability and writing skills.
CO2: Identify essential parameters of each section of research articles.
CO3: Apply the knowledge for writing and submit research paper for publication.
CO4: Develop skills that are required to maintain quality of research paper.

UNIT-I: Research paper Writing Skills Part-I
Planning and Preparation, Word Order, Breaking up long sentences, Structuring, Paragraphs and Sentences, Being Concise, and Removing Redundancy

UNIT-II: Research paper Writing Skills Part-II
Avoiding Ambiguity and Vagueness, Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticising, Paraphrasing and Plagiarism

UNIT-III: Parts of research Paper
Title, Abstract, Introduction, Review of the Literature, Methods, Results, Discussion, Conclusions, the Final Check.

UNIT-IV: Preparation of manuscript
Key skills are needed when writing a Title, an Abstract, an Introduction, a Review of the Literature, the Methods, the Results, the Discussion, Conclusions, preparing the tables and figures

UNIT-V: Publishing the Paper
Rights and Permission, How to Submit the Manuscript, The Review Process (How to Deal with Editors), The Publishing Process (How to Deal with Proofs) and After Publication.

Text Books:
Pre-Requisites: ECAD Lab

COURSE EDUCATIONAL OBJECTIVES:
In this course student will learn about the VHDL Programming of various Digital Circuits, design and implementation of various CMOS IC circuits using Mentor Graphics Tools.

COURSE OUTCOMES: At the end of this course student will be able to
CO1: Design CMOS Logic gates using Pyxis Schematic Editor.
CO2: Model digital modules using VHDL/Verilog and Simulate.

Syllabus:
➢ Minimum of 10 programs from Part –I and 2 programs from Part -II are to be conducted.
➢ Design and implementation of the following CMOS digital circuits using Mentor Graphics /Xilinx CAD tools. The design shall include Gate-level design, Transistor-level design, Hierarchical design, Verilog HDL/VHDL design, Logic synthesis, Simulation and verification.

Part –I: VLSI Front End Design programs:
Programming can be done using any complier. Down load the programs on FPGA/CPLD boards and performance testing may be done using pattern generator (32 channels) and logic analyzer apart from verification by simulation with any of the front end tools.
1. Design of 8 input priority encoder and 3 to 8 Decoder
2. Design of 8x1Mux and 1x8 Demux
3. Design of 4 bit adder
4. Design 4 bit Magnitude Comparator
5. Design of BCD adder
6. Design of ALU
7. Design of D,T,JK Flip Flops
8. Design of Shift Registers
9. Design of Counters
10. Design of FSM (Moore’s, Mealy Machines)
11. Design of Booth multiplier
12. Design of Electronic Dice game

Part –II: VLSI Back End Design programs:
➢ Design and implementation of the following CMOS digital/analog circuits using Cadence / Mentor Graphics / Synopsys / Equivalent CAD tools.
➢ The design shall include Gate-level design/Transistor level design/Hierarchical design/Verilog HDL or VHDL design, Logic synthesis, Simulation and verification, Scaling of CMOS Inverter for different technologies, study of secondary effects (temperature, power supply and process corners), Circuit optimization with respect to area, performance and/or power, Layout, Extraction of parasitics and back annotation,
modifications in circuit parameters and layout consumption, DC/transient analysis, Verification of layouts (DRC, LVS).

1. Introduction to layout design rules

2. Layout, physical verification, placement & route for complex design, static timing analysis, IR drop analysis and crosstalk analysis of the following:
   - Basic logic gates
   - CMOS inverter
   - CMOS NOR/ NAND gates
   - CMOS XOR and MUX gates
   - CMOS 1-bit full adder
   - Static / Dynamic logic circuit (register cell)
   - Latch
   - Pass transistor

3. Layout of any combinational circuit (complex CMOS logic gate)- Learning about data paths
Pre-Requisites: Microprocessors and Microcontrollers Lab

COURSE EDUCATIONAL OBJECTIVES:
In this course student will learn about the programming in Assembly language programs on ARM processor kits, programming on CPLD and FPGA kits using EDK Tools.

COURSE OUTCOMES:
At the end of this course student will be able to
CO1: Develop the Assembly Language Programs for ARM processors.
CO2: Develop the interfacing programs for ARM processors and I/O devices.
CO3: Design an Embedded System using the FPGA and EDK tools.

Syllabus:

**Part I**
- The following programs are to be implemented on **ARM based Processors/Equivalent**.
- **Minimum of 10 programs are to be conducted.**

  1. ARM Assembly Language Programming-I
  2. ARM Assembly Language Programming-II
  3. Program to Interface 8 Bit LED
  4. Program to demonstrate Time delay program using built in Timer/Counter feature
  5. Program to Displaying a message in a 2 line x 16 Characters LCD display and verify the result in debug terminal.
  6. Generation of PWM Signal
  7. Serial Communication
  8. Traffic light Controller
  9. Stepper motor Controller
  10. Basic Audio Processing on IDE environment.
  11. Program to demonstrate I2C Interface on IDE environment
  12. Program to implement Buzzer Interface on IDE environment

**Part II**
The following programs are to be implemented on **Xilinx FPGA Zynq 7000 series/Equivalent.**
- **Minimum of 2 programs are to be conducted.**

  14. Design dual processor based System on chip using Xilinx EDK Tools and Zynq 7000 series FPGA.
  15. Hardware Software co-design using Xilinx EDK Tools and Advanced FPGA Board Zynq 7000 series.
M. Tech (VLSI & Embedded Systems)
II – Semester Detailed Syllabus
M. Tech. (II Sem.)  23VE09 – ANALOG VLSI DESIGN

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PRE-REQUISITES: VLSI Design

COURSE EDUCATIONAL OBJECTIVES:
In this course student will learn about the operation of MOS devices, design of Oscillators, Phase Locked Loops, Reference Generators and Data Converters.

COURSE OUTCOMES: At the end of the course, student will be able to
CO1: Understand the basic physics and operation of MOS devices.
CO2: Develop efficient analytical tools for quantifying the behavior of basic circuits by inspection.
CO3: Design of Oscillators and Phase Locked Loops.
CO4: Develop reference generators.
CO5: Implement efficient data converters.

UNIT I:
**Basic MOS Device Physics:** General considerations, MOS I/V Characteristics, second order effects, MOS device models.

**Single stage Amplifier:** CS stage with resistance load, divide connected load, current source load, triode load, CS stage with source degeneration, source follower, common-gate stage, cascade stage, choice of device models.

UNIT II:
**Frequency response of CS stage:** source follower, Common gate stage, Cascade stage and Difference pair. Noise in CS stage, C- G stage, source follower, cascade stage, differential pair.

**Differential Amplifiers & Current Mirrors:** Basic difference pair, common mode response, Differential pair with MOS loads, Gilbert cell. Basic current mirrors, Cascade mirrors, active current mirrors.

UNIT III:

**Oscillators and Phase Locked Loops:** Ring Oscillators, LC Oscillators, VCO, Mathematical Model of VCO. Simple PLL, Charge pump PLL, Non-ideal effects in PLL, Delay locked loops and applications.

UNIT IV:
**Band gap References** and Switched capacitor Circuits: General Considerations, Supply Independent biasing, PTAT Current Generation, Constant Gm Biasing, Sampling Switches, Switched Capacitor Amplifiers.

UNIT V:
**Data Converter Architectures:** DAC & ADC Specifications, Resistor String DAC, R-2R Ladder Network, Current Steering DAC, Charge Scaling DAC, Cyclic DAC, Pipeline DAC, Flash ADC, Pipeline ADC, Integrating ADC, Successive Approximation ADC.
TEXT BOOK:

REFERENCE BOOK:
M. Tech. (II Sem.) 23VE10 – REAL TIME OPERATING SYSTEMS

PRE-REQUISITES: Embedded System Design

COURSE EDUCATIONAL OBJECTIVES:
In this course student will learn about fundamental concepts of real time operating systems, operating system objects, services and I/O concepts, various interrupts and timers.

COURSE OUTCOMES: At the end of the course, student will be able to
CO1 Understand the basic set of commands and utilities in Linux/UNIX systems.
CO2 Explain the fundamental concepts of real-time operating systems.
CO3 Analyze real-time operating systems objects, services and I/O concepts.
CO4 Evaluate various Interrupts and Timers.
CO5 Design real time embedded systems using the concepts of RTOS.

UNIT – I:
Introduction: Introduction to UNIX/LINUX, Overview of Commands, File I/O (open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

UNIT - II:

UNIT - III:
Objects, Services and I/O Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem

UNIT - IV:

UNIT V:
RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, Tiny OS, and Basic Concepts of Android OS.

TEXT BOOKS:

REFERENCE BOOKS:
1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2007, TMH.
2. Advanced UNIX Programming, Richard Stevens
3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh
Pre-Requisites: Basics on CPLD and FPGA

COURSE EDUCATIONAL OBJECTIVES:
In this course student will learn about the complex programmable logic devices, field programmable gate arrays, architecture of SRAM programmable and anti-fuse programmed FPGAs.

COURSE OUTCOMES: At the end of this course student will be able to
CO1 Analyze different types of Complex Programmable Logic Devices.
CO2 Understand different types of Field Programmable Gate Arrays.
CO3 Evaluate architecture of SRAM Programmable FPGAs.
CO4 Explain the device Architecture of Anti-Fuse Programmed FPGAs.
CO5 Design the application for Combinational and Sequential Circuits.

UNIT - I:
Introduction to Programmable Logic Devices:
Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic.

UNIT – II:

UNIT – III:
Field Programmable Gate Arrays:
Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, and Programmable I/O blocks in FPGAs, Dedicated specialized Components of FPGAs, and Applications of FPGAs.

UNIT – IV:
SRAM Programmable FPGAs:
Anti-Fuse Programmed FPGAs:
Introduction, Programming Technology, Device Architecture, TheActel ACT1, ACT2 and ACT3 Architectures.

UNIT – V:
Design Applications:
General Design Issues, Counter Examples, A Fast Video Controller, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXTBOOKS
REFERENCES:
1. Field Programmable Gate Arrays by John V. Oldfield, Richard C. Dorf, Wiley India.
3. Digital Systems Design with FPGAs and CPLDs by Ian Grout, Elsevier, Newnes.
PRE-REQUISITES: Embedded Systems and Operating Systems

COURSE EDUCATIONAL OBJECTIVES:
In this course student will learn about Operating systems concepts, programming concepts, programming in Linux and RT Linux.

COURSE OUTCOMES: At the end of the course, student will be able to
CO1  Understand the basic concepts of Operating Systems.
CO2  Explain the Programming concepts of RTOS.
CO3  Analyze various Case Studies for practical applications.
CO4  Create Target Image for Windows XP Embedded & write Programming in Linux.
CO5  Write Programming in RT Linux.

UNIT-I: Introduction

UNIT-II: RTOS Programming
Basic Functions and Types of RTOS for Embedded Systems, RTOS mCOS-II, RTOS Vx Works, Programming concepts of above RTOS with relevant Examples, Programming concepts of RTOS Windows CE, RTOS OSEK, RTOS Linux 2.6.x and RTOS RT Linux.

UNIT-III: Program Modeling – Case Studies
Case study of embedded system design and coding for an Automatic Chocolate Vending Machine (ACVM) Using Mucos RTOS, case study of digital camera hardware and software architecture, case study of coding for sending application layer byte streams on a TCP/IP Network Using RTOS Vx Works, Case Study of Embedded System for an Adaptive Cruise Control (ACC) System in Car, Case Study of Embedded System for a Smart Card, Case Study of Embedded System of Mobile Phone Software for Key Inputs.

UNIT-IV: Target Image Creation & Programming in Linux

UNIT-V: Programming in RT Linux
Overview of RT Linux, Core RT Linux API, Program to display a message periodically, semaphore management, Mutex, Management, Case Study of Appliance Control by RT Linux System.
TEXT BOOKS:

REFERENCES:
PRE-REQUISITES: None

COURSE EDUCATIONAL OBJECTIVES:
In this course student will learn about testable design, test generation algorithms for combinational and sequential circuits, design verification and verification tools, timing and physical design verification.

COURSE OUTCOMES: At the end of the course, student will be able to
CO1 Identify the significance of testable design
CO2 Implement combinational and sequential circuit test generation algorithms
CO3 Understand the importance of Design verification.
CO4 Learn verification tools.
CO5 Analyze the static timing verification and physical design verification.

UNIT I:
Test Generation for Combinational Logic Circuits: Fault Diagnosis of Digital Circuits, Test Generation Techniques for Combinational Circuits, Detection of Multiple Faults in Combinational Logic Circuits.

UNIT II:

UNIT III:
Testable Memory Design: RAM Fault Models, Test Algorithms for RAMs, Detection of Pattern Sensitive Faults, BIST Techniques for Ram Chips, Test Generation and BIST for Embedded RAMs.
Importance of Design Verification: What is verification? What is attest bench? The importance of verification, Reconvergence model, Formal verification, Equivalence checking, Model checking, Functional verification.[Ref4- Chapter1]

UNIT IV:
Verification Tools: Linting tools: Limitations of linting tools, lintingverilog source code, linting VHDL source code, lintingOpenVera and esource code, code reviews. Simulators: Stimulus and response, Event based simulation, cycle based simulation, Co-simulators, verification intellectual property: hardware modelers, waveform viewers.[Ref4-Chapter2]
The verification plan: The role of verification plan: specifying the verification plan, defining the first success. Levels of verification: unit level verification, reusable components verification, ASIC and FPGA verification, system level verification, board level verification, verifying strategies, verifying responses. [Ref4-Chapter3]
UNIT V:
Static Timing Verification: Concept of static timing analysis. Cross talk and noise. Limitations of STA. slew of a waveform, Skew between the signals, Timing arcs and unateness, Min and Max timing paths, clock domains, operating conditions, critical path analysis, falsepaths, Timing models. [Ref5 Chapter 1, 2, 3, 8]
Physical Design Verification: Layout rule checks and electrical rule checks. Parasitic extraction. Antenna, Crosstalk and Noise: Cross talk glitch analysis, crosstalk delay analysis, timing verification [Ref6 Chapter 8]

TEXT BOOKS:

REFERENCE BOOKS:
PRE-REQUISITES: Communication Systems

COURSE EDUCATIONAL OBJECTIVES:
In this course student will learn about wireless components, wireless networks, wireless system architecture, protocols, Mobile IP, Adhoc networks, digital audio and video broadcasting for high speed internet access.

COURSE OUTCOMES: At the end of the course, student will be able to
CO 1: Discuss about wireless components and wireless networks.
CO 2: Describe System architecture and medium access control protocols.
CO 3: Explain Mobile IP and mobile Adhoc networks.
CO 4: Compare different transport layer protocols.
CO 5: Analyze requirements of digital audio and video broadcasting for high-speed internet access.

UNIT I

UNIT II:
(Wireless) Medium Access Control: Motivation for a specialized MAC (Hidden and exposed terminals, Near and far terminals), SDMA, FDMA, TDMA, CDMA.

UNIT III:
Mobile Network Layer:
Mobile IP: Goals, assumptions, entities and terminology, IP packet delivery, agent advertisement and discovery, registration, tunneling and encapsulation, optimizations, Dynamic Host Configuration Protocol (DHCP).
Mobile Ad hoc Networks (MANETs): Overview, Properties of a MANET, spectrum of MANET applications, routing and various routing algorithms.

UNIT IV
Mobile Transport Layer:Traditional TCP, Indirect TCP, Snooping TCP, Mobile TCP, Fast retransmit/fast recovery, Transmission /time-out freezing, Selective retransmission, Transaction oriented TCP.

UNIT V
TEXT BOOK:

REFERENCE BOOKS:
PRE-REQUISITES: CPLD & FPGA

COURSE EDUCATIONAL OBJECTIVES:  
In this course student will learn about ASIC design flow, architecture of ASIC library design, programmable ASIC logic cells, logic synthesis and physical design phases.

COURSE OUTCOMES: At the end of the course, student will be able to  
CO1: Acquire Knowledge on ASIC design flow  
CO2: Analyze the architecture of ASIC library designs  
CO3: Understanding the programmable ASIC logic cells  
CO4: Analyzing the Logic synthesis in HDLs  
CO5: Comprehend the physical design phases

Unit I: Types of ASICs – Design flow – Economics of ASICs – ASIC cell libraries – CMOS logic: CMOS Transistors, The CMOS process, CMOS design rules, Combinational logic cells, sequential logic cells, data path logic cells – I/O cells – cell compilers.

Unit II: ASIC Library design: Transistors as resistors – parasitic capacitance – logical effort, library cell design, library architecture, gate array design, standard cell design, data path cell design programmable ASICs: The Anti-fuse, Static RAM, EPROM and EEPROM Technology, practical issues, specifications.


Unit IV: Logic synthesis in Verilog and logic synthesis in VHDL, Finite –State machine synthesis, Memory synthesis, performance-Driven synthesis, Simulation: Types of simulation, The Comparator/MUX example, logic systems, how logic simulation works, cell models, delay models, Static Timing Analysis, formal verification, switch-level simulation, transistor level simulation.


TEXT BOOKS:  
REFERENCES:
PRE-REQUISITES: DSP

COURSE EDUCATIONAL OBJECTIVES:
In this course student will learn about the fundamentals of VLSI signal processing and expose them to examples of applications. Design and optimize VLSI architectures for basic DSP algorithms.

COURSE OUTCOMES: At the end of the course, student will be able to
CO1: Understand VLSI design methodology for signal processing systems.
CO2: Differentiate between folding and unfolding architectures.
CO3: Elaborate various Systolic Array structures.
CO4: Analyze the VLSI algorithms and architectures for DSP.
CO5: Implement basic architectures for DSP using CAD tools.

UNIT -I:
Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms

UNIT -II:

UNIT -III:

UNIT -IV:

UNIT -V:

TEXT BOOKS:
REFERENCE BOOKS:
Pre-requisites: Nil

Course Educational Objectives:
- To enable the student to understand the importance of constitution.
- To understand the structure of Executive, Legislature and Judiciary.
- To understand Philosophy of fundamental rights and duties.
- To understand the autonomous nature of constitution bodies like Supreme Court and High Court Controller and Auditor General of India and Election Commission of India.
- To understand the Central and State relation, financial and administrative.

Course Outcomes: At the end of the course, the student shall be able to
CO1: Understand history and philosophy of constitution with reference to Preamble, Fundamental Rights and Duties (Understand – L2).
CO2: Understand the concept of Unitary and Federal Government along with the role of President, Prime Minister and Judicial System (Understand – L2).
CO3: Understand the structure of the state government, Secretariat, Governor and Chief Minister and their functions (Understand – L2).
CO4: Learn local administration viz. Panchayat, Block, Municipality and Corporation (Understand – L2).
CO5: Learn about Election Commission and the process and about SC, ST, OBC and women (Understand – L2).

UNIT – I:

UNIT – II:
Union Government and its Administration Structure of the Indian Union: Federalism Centre – State relationship, President: Role, Power and Position. Prime Minister (PM) and Council of Ministers, Cabinet and Central Secretariat, Lok Sabha, Rajya Sabha. The Supreme Court and High Court: Powers and Functions.

UNIT – III:
State Government and its Administration Governor – Role and Position – Chief Minister (CM) and Council of Ministers. State Secretariat: Organization, Structure and Functions.

UNIT – IV:
A Local Administration -- Role and Importance, Municipalities – Mayor and Role of Elected Representative, Panchayati Raj: Functions of Panchayati Raj Institution, Zilla Panchayat, Elected Officials and their roles, Village level – Role of Elected and Appointed officials.

UNIT – V:
Reference Books:
3. J. A. Siwach, Dynamics of Indian Government and Politics.

E-Resources:
1. nptel.ac.in/courses/109104074/8.
2. nptel.ac.in/courses/109104045.
3. nptel.ac.in/courses/101104065.
PRE-REQUISITES: PSPICE knowledge

COURSE EDUCATIONAL OBJECTIVES:
In this course student will learn about the design of basic building blocks of analog VLSI chips, cascade amplifiers and operational trans-conductance amplifier using CMOS technology.

COURSE OUTCOMES: At the end of the course, student will be able to
CO1: Design basic building blocks of analog VLSI Chips
CO2: Design cascade amplifier using CMOS Technology
CO3: Design operational Trans-conductance amplifier (OTA) using CMOS Technology

Minimum of 10 experiments are to be conducted using Cadence/Mentor Graphics/Synopsys/Equivalent CAD Tools

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<td>1.</td>
<td>Transconductance plots (voltage bias, current bias and technology bias).</td>
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<td>2.</td>
<td>Design of basic amplifier.</td>
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<td>3.</td>
<td>Design of cascode amplifier.</td>
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<td>4.</td>
<td>Design of basic current sink.</td>
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<td>5.</td>
<td>Design current sink by using negative feed back resistor.</td>
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<td>6.</td>
<td>Design of cascode current sink.</td>
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<td>7.</td>
<td>Design of positive feed back boot strap current sink.</td>
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<td>8.</td>
<td>Design of regulated cascode current sink.</td>
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<td>10.</td>
<td>Design of cascode current mirror.</td>
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PRE-REQUISITES: Knowledge on Operating Systems

COURSE EDUCATIONAL OBJECTIVES:
In this course student will learn about multitasking applications using RTOS, porting Linux on FPGA and create applications using ARM’s Real Time Operating system.

COURSE OUTCOMES:
At the end of the course, student will be able to
CO1: Develop multitasking applications using RTOS
CO2: Porting Linux on Zynq FPGA to develop embedded applications
CO3: Create applications using ARM’s Real Time Operating System RTX

Minimum of 10 experiments are to be conducted using Xilinx EDK/ MicroVision IDE Keil
Write the following programs to understand the use of RTOS with ARM Processor on IDE Environment using ARM Tool chain and Library:

1. Create an application that creates two tasks that wait on a timer whilst the main task loops.
2. Write an application that creates a task which is scheduled when a button is pressed, which illustrates the use of an event set between an ISR and a task
3. Write an application that Demonstrates the interruptible ISRs(Requires timer to have higher priority than external interrupt button)
4. a). Write an application to Test message queues and memory blocks.
   b). Write an application to Test byte queues
5. Write an application that creates two tasks of the same priority and sets the time slice period to illustrate time slicing.

Interfacing Programs:
6. Write an application that creates a two task to Blinking two different LEDs at different timings
7. Write an application that creates a two task displaying two different messages in LCD display in two lines.
8. Sending messages to mailbox by one task and reading the message from mailbox by another task.
9. Sending message to PC through serial port by three different tasks on priority Basis.
10. Porting Linux and developing simple application on Xilinx Zed board
11. Developing image processing application with Linux OS on Xilinx Zynq FPGA
12. Simulating a stepper-motor driver
13. Write simple applications using RTX (ARM Keil’s real time operating system, RTOS).
M. Tech (VLSI & Embedded Systems)
III – Semester Detailed Syllabus
PRE-REQUISITES: Operating Systems & Linux

COURSE EDUCATIONAL OBJECTIVES:
In this course student will learn about embedded Linux, desktop Linux, embedded drivers for embedded applications, operating system porting, Linux real time programming.

COURSE OUTCOMES: At the end of the course, student will be able to
CO1: Compare Embedded Linux, desktop Linux and Embedded Linux distributions
CO2: Develop board support packages for optimized embedded storage space
CO3: Choose embedded drivers for typical embedded application
CO4: Analyze application porting and operating system porting
CO5: Describe Real-Time programming in linux /Hard Real-Time Linux

UNIT – I:

UNIT – II:
Embedded Storage: Flash Map, MTD—Memory Technology Device, MTD Architecture, Flash-Mapping Drivers, MTD Block and Character devices, Embedded File systems, Optimizing Storage Space.

UNIT – III:

UNIT-IV:
Porting Applications: Architectural Comparison, Application Porting Road Map, Programming with Pthreads, Operating System Porting Layer (OSPL), Kernel API Driver.

Unit-V:

TEXT BOOK:

REFERENCE BOOK:
1. Embedded Linux – Hardware, Software and Interfacing
PRE-REQUISITES: None

COURSE EDUCATIONAL OBJECTIVES:
In this course student will learn about Micro-systems, Micro-fabrication. Mechanics for MEMS design, Electrostatic actuators and Electromagnetic actuators, various sensor structures.

COURSE OUTCOMES: At the end of the course, student will be able to
CO1: Describe MEMS, Microsystems and Micro-fabrication
CO2: Analyze mechanics for MEMS Design
CO3: Distinguish Electrostatic actuators and Electromagnetic actuators
CO4: Model various circuits for MEMS Design
CO5: Choose Micro-bridge gas sensors, Piezo resistive Pressure Sensor and Bio-Chemical Sensors

UNIT – I: INTRODUCTION TO MEMS

UNIT – II: MECHANICS FOR MEMS DESIGN
Elasticity, stress, strain and material properties, Bending of thin plates, Spring configurations, torsional deflection, Mechanical vibration, Resonance - Thermo mechanics – Actuators, force and response time, Fracture and thin film mechanics, material, Physical Vapor Deposition (PVD), Chemical Mechanical Polishing (CMP).

UNIT – III: ELECTROSTATIC DESIGN
Electrostatics:- basic theory, electro static instability, Surface tension, gap and finger pull up - Electro static actuators - Comb generators - Gap closers - Rotary motors - Inch worms - Electromagnetic actuators - Bistable actuators.

UNIT – IV: CIRCUIT MODELING OF MEMS

UNIT – V: CASE STUDIES

TEXT BOOK:
REFERENCE BOOKS:
PRE-REQUISITES: VLSI Design

COURSE EDUCATIONAL OBJECTIVES:
In this course student will learn about concepts of power consumption, power analysis, low power design, and low power architectural level methodologies.

COURSE OUTCOMES: At the end of the course, student will be able to
CO1: Understand the concepts of power consumptions
CO2: Analyze the power analysis
CO3: Create low power design circuits
CO4: Comprehend the low power systems
CO5: Evaluate the Architectural Level Methodologies

UNIT I:
Introduction: Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches, Physics of power dissipation in CMOS devices.

UNIT II:
Power estimation, Simulation Power analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation.
Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

UNIT III:
Low Power Design Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library.
Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic.

UNIT IV:
Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.
Low power Clock Distribution: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network.

UNIT V:

TEXT BOOK:
REFERENCE BOOKS:
Open Elective Courses offered to other Departments
Open Elective

M. Tech. (III Sem.)

23VE81 – CAD FOR VLSI DESIGN

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Pre-Requisites: VLSI Design

COURSE EDUCATIONAL OBJECTIVES:
In this course student will learn about the design cycles, various techniques on Partitioning, Placement and Routing and addressing their problems.

COURSE OUTCOMES: At the end of this course student will be able to
CO1: Identify the need of CAD for VLSI design.
CO2: Analyze VLSI design algorithms for partitioning.
CO3: Formulate placement, floor planning and pin assignment problems and simulate.
CO4: Resolve routing issues using various algorithms.
CO5: Illustrate physical design cycle for FPGAs.

UNIT I:
VLSI Physical Design Process: Introduction, VLSI Design cycle, new trends in VLSI design cycle, new trends in Physical design cycle, Design styles, full custom Basic terminology, complex issues, basic algorithms, Basic data structures, and algorithms.

UNIT II:

UNIT III:
Placement, Floor Planning & Pin Assignment: problem formulation, simulation base placement algorithms, other placement algorithms, constraint based floor planning, floor planning algorithms for mixed block & cell design. General & channel pin assignment

UNIT IV:
Global Routing: Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches
Detailed Routing: Problem formulation, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms.
Over The Cell Routing & Via Minimization: two layers over the cell routers, constrained & unconstrained via minimization

UNIT V:
Physical Design of FPGAs:
Introduction, FPGA Technologies, Physical design cycle for FPGAs, Partitioning, Routing, Routing algorithms for the non-segmented model, Routing algorithms for segmented model, routing algorithms for staggered model.

TEXT BOOK:
REFERENCE BOOKS:
Pre-requisites: Digital System Design

Course Educational Objectives: This course enlightens the knowledge on simple Programmable logic devices, Complex Programmable Logic Devices, Field Programmable Gate Arrays, ASICs, ASIC library designs and ASIC programming technologies.

Course Outcomes (COs): At the end of this course, student will be able to

| CO1 | Understand the various types of Programmable Logic Devices |
| CO2 | Analyze the architectures of Field Programmable Gate Arrays and ASICs |
| CO3 | Evaluate the Programmable Logic Devices |
| CO4 | Design of Application Specific Integrated Circuit libraries. |

UNIT – I
Introduction to Programmable Logic Devices: Review of simple PLDs, Complex Programmable Logic Devices, Field Programmable Gate Arrays, Advantages fo FPGAs, Designing of FPGAs, Technology trends.

UNIT – II
Programming Techniques of FPGAs: Introduction, SRAM Programming, Device architecture, design trade-offs, Xilinx XC2000, XC3000, XC4000 architectures, automated design implementations, technology specific synthesis, Antifuse programming technology, Device architectures, Routing architectures of FPGAs, Act1, Act2, Act3, Programming and testing.

UNIT – III
Introduction to ASICS: Full-custom ASICs, Standard Cell-based ASICs, Gate-Array based ASICs, Design flow, Economics of ASICs, Comparison between ASIC technologies, ASIC Cell Libraries.

UNIT – IV
ASIC Library Design: Transistors as Resistors, Transistor Parasitic Capacitance, Logical effort, Library cell design, Library architecture, Gate Array Design, Standard Cell Design, Data path Cell Design, EPROM and EEPROM technology.

UNIT – V
Programmable ASIC Logic Cells: Actel ACT, Xilinx, LCA, Altera FLEX, Altera MAX.
Programmable ASIC I/O Cells: DC and AC inputs and outputs, Clock input, Power inputs, Xilinx I/O blocks, Other I/O Cells.

TEXT BOOK
REFERENCE
Open Elective
23VE83 – VLSI TESTING

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**PRE-REQUISITES:** None

**COURSE EDUCATIONAL OBJECTIVES:**
In this course student will learn about testable design, test generation algorithms for combinational and sequential circuits, testable memory design.

**COURSE OUTCOMES:** At the end of the course, student will be able to

- **CO1** Identify the significance of testing and testable design.
- **CO2** Implement combinational and sequential circuit test generation algorithms.
- **CO3** Apply the built-in self test algorithms to identify the faults in VLSI circuits.
- **CO4** Analyze the memory faults using memory testing algorithms.

**UNIT I:**
**Introduction to Testing:** Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing. Faults in Digital Circuits: Failures and Faults, Modeling of Faults – Stuck-At faults, Bridging faults, Delay faults, Breaks and Transistor Stuck-On / Open faults; Temporary Faults.

**UNIT II:**
**Test Generation for Combinational Logic Circuits:** Fault Diagnosis of Digital Circuits, Test Generation Techniques for Combinational Circuits – One-Dimensional Path Sensitization, D-Algorithm, PODEM, FAN, Delay Fault Detection; Detection of Multiple Faults in Combinational Logic Circuits.

**UNIT III:**
**Design of Testable Sequential Circuits:** Controllability and Observability, Ad Hoc Design Rules for Improving Testability, Design of Dignosable Sequential Circuits, The Scan-Path Technique for Testable Sequential Circuit Design, Level-Sensitive Scan Design, Random Access Scan Technique, Partial Scan, Testable Sequential Circuit Design Using Nonscan Techniques, CrossCheck, Boundary Scan.

**UNIT IV:**
**Built-In Self Test:** Test Pattern Generation for BIST – Exhaustive Testing, Pseudo-Exhaustive Pattern Generation, Pseudo-Random Pattern Generator, Deterministic Testing; Output Response Analysis – Transition Count, Syndrome Checking, Signature Analysis; Circular BIST, BIST Architectures – BILBO (Built-In Logic Block Observer), STUMPS (Self-Testing Using an MISR and Parallel Shift Register), LOCST (LSSD On-Chip Self-Test).

**UNIT V:**
**Testable Memory Design:** RAM Fault Models, Test Algorithms for RAMs – GALPAT (Galloping 0s and 1s), Walking 0s and 1s, March Test, Checkerboard Test; Detection of Pattern Sensitive Faults, BIST Techniques for Ram Chips, Test Generation and BIST for Embedded RAMs.

**TEXT BOOKS:**
REFERENCE BOOKS: