## COURSE STRUCTURE

### I SEMESTER

<table>
<thead>
<tr>
<th>Subject code</th>
<th>Name of the Subject</th>
<th>Contact hours/week</th>
<th>Credits</th>
<th>Scheme of Valuation</th>
<th>Total Marks</th>
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<tr>
<td>MTLV101</td>
<td>VLSI Technology and Design</td>
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<td>MTLV102</td>
<td>CPLD and FPGA Architectures and Applications</td>
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<td>Program Elective-I Wireless Communications &amp; Networks</td>
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<td>Nano Electronics</td>
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<td>Embedded Linux and Basics of Device Drivers</td>
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### III & IV SEMESTERS

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**Signature:**

**HEAD**

Department of Electronics & Communication Engineering
Lakireddy Bali Reddy College of Engineering
LAVARAM, Krishna Dt., Andhra Pradesh

M.TECH.(VLSI and ES)  A.Y. 2016-17  Page 12 of 41
I SEMESTER
MTVL101-VLSI TECHNOLOGY AND DESIGN

Lecture : 4 Periods/week

Internal Marks : 40

External Marks : 60

Credits : 3

External Examination : 3 Hrs

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UNIT-I:

UNIT-II

UNIT-III
Combinational Circuit Design: Delay Estimation, Logical Effort and Transistor Sizing, Power Dissipation, Circuit Families, Circuit Pitfalls, Low-power Logic Design, Comparison of Circuit Families, Silicon-on-Insulator Circuit Design

UNIT-IV

UNIT-V
Floor Planning and System Design: Floor planning methods, Global interconnect, Floor Plan design, off-chip connections, Register Transfer Design, Pipelining

TEXT BOOKS

REFERENCES
MTVL103 - MICRO CONTROLLERS FOR EMBEDDED SYSTEM DESIGN

Lecture : 4 Periods/week
Internal Marks : 40
External Marks : 60
Credits : 3
External Examination : 3 Hrs

UNIT – I

UNIT – II

UNIT – III
PIC Microcontroller Hardware: Introduction, Architectural overview, Memory organization, interrupts and reset, I/O ports, Timers

UNIT – IV
ARM Architecture: ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families.

Unit – V
Device Drivers & Interrupt service Mechanism: Programmed-I/O Busy-wait approach without ISM,ISR concept, Interrupt sources, Interrupt service mechanism, Multiple Interrupts, context and the periods for context switching, Interrupt latency and deadline, Classification of processors ISM from context-saving angle, Direct Memory Access, Device driver programming, Serial Bus communication protocols

TEXT BOOKS

REFERENCE BOOKS
MTVL102-CPLD AND FPGA ARCHITECTURE AND APPLICATIONS

Lecture : 4 Periods/week
Credits : 3

Internal Marks : 40
External Marks : 60
External Examination : 3 Hrs

UNIT - I

UNIT – II
Field Programmable Gate Arrays: Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, and Programmable I/O blocks in FPGAs, Dedicated specialized Components of FPGAs, and Applications of FPGAs.

UNIT – III

UNIT – IV
Anti-Fuse Programmed FPGAs: Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT – V
Design Applications: General Design Issues, Counter Examples, A Fast Video Controller, A position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXTBOOKS

REFERENCE BOOKS
1. Field Programmable Gate Arrays by John V. Oldfield, Richard C. Dorf, Wiley India.
3. Digital Systems Design with FPGAs and CPLDs by Ian Grout, Elsevier, Newnes.
MTVL104-EMBEDDED REAL TIME OPERATING SYSTEMS

Lecture : 4 Periods/week

Internal Marks : 40

External Marks : 60

Credits : 3

External Examination : 3 Hrs

UNIT – I
Introduction: Introduction to UNIX/LINUX, Overview of Commands, File I/O (open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

UNIT - II

UNIT - III
Objects, Services and I/O
Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem

UNIT - IV

UNIT V
RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, Tiny OS, and Basic Concepts of Android OS.

TEXT BOOK

REFERENCE BOOKS
1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2007, TMH.
2. Advanced UNIX Programming, Richard Stevens
3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh

Department of Electronics & Communication Engineering
Lakireddy Bali Reddy College of Engineering

A.Y. 2016-17 Page 17 of 41
MTVL1051 - WIRELESS COMMUNICATIONS AND NETWORKS

<table>
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UNIT-I

**Wireless Communications & System Fundamentals:** Introduction to wireless communications systems, examples, comparisons & trends, Cellular concepts-frequency reuse, strategies, interference & system capacity, trucking & grade of service, improving coverage & capacity in cellular systems.

UNIT-II

**Multiple Access Techniques for Wireless Communication:** FDMA, TDMA, SSMA (FHMA/CDMA/Hybrid techniques), SDMA technique (AS applicable to wireless communications). Packet radio access-protocols, CSMA protocols, reservation protocols, capture effect in packet radio, capacity of cellular systems.

UNIT-III

**Wireless Networking:** Introduction, differences in wireless & fixed telephone networks, traffic routing in wireless networks – circuit switching, packet switching X.25 protocol. **Wireless data services** – cellular digital packet data (CDPD), advanced radio data information systems, RAM mobile data (RMD). Common channel signaling (CCS), ISDN-Broad band ISDN & ATM, Signaling System no .7 (SS7)-protocols, network services part, user part, signaling traffic, services & performance

UNIT-IV

**Mobile IP and Wireless Application Protocol:** Mobile IP Operation of mobile IP, Co-located address, Registration, Tunneling, WAP Architecture, overview, WML scripts, WAP service, WAP session protocol, wireless transaction, Wireless datagram protocol.

**Wireless LAN Technology** Infrared LANs, Spread spectrum LANs, Narrow bank microwave LANs, IEEE 802 protocol Architecture, IEEE802 architecture and services, 802.11 medium access control, 802.11 physical layer.

UNIT-V

**Mobile Data Networks:** Introduction, Data oriented CDPD Network, GPRS and higher data rates, Short messaging service in GSM, Mobile application protocol.

**Ad-hoc Wireless Networks:** Cellular and Adhoc wireless networks, applications, MAC protocols, Routing, Multicasting, Transport layer Protocols, quality of service browsing, deployment considerations, Adhoc wireless Internet

TEXT BOOKS


REFERENCES

1. Wireless Digital Communications – Kamilo Feher, 1999, PHI.
MTVL1052-VLSI DESIGN AUTOMATION

Lecture : 4 Periods/week  Internal Marks : 40
External Marks : 60
Credits : 4  
External Examination : 3 Hrs

UNIT-I
Logic Synthesis & Verification: Introduction to combinational logic synthesis, Binary Decision Diagram, Hardware models for High-level synthesis.

UNIT-II

UNIT-III
Placement, Floor Planning & Pin Assignment : Problem formulation, simulation base placement algorithms, other placement algorithms, constraint based floor planning, floor planning algorithms for mixed block & cell design. General & channel pin assignment.

UNIT-IV
Global Routing: Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches
Detailed Routing: problem formulation, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms.
Over The Cell Routing & Via Minimization: two layers over the cell routers, constrained & unconstrained via minimization

UNIT-V
Scripting Languages: Overview of Scripting Languages – PERL, CGI, VB Script, Java Script. PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables. Inter process Communication Threads, Compilation & Line Interfacing

TEXT BOOKS

REFERENCE BOOKS
MTVL1053-NANO ELECTRONICS

Lecture : 4 Periods/week  
Internal Marks : 40

Credits : 3  
External Marks : 60

External Examination : 3 Hrs

UNIT-I

UNIT-II
Characterization: Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, spectroscopy techniques: photon, radiofrequency, electron, surface analysis and depth profiling: electron, mass, Ion beam, Reflectometry, Techniques for property measurement: mechanical, electron, magnetic, thermal properties.


UNIT-III
Fabrication techniques: requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching, cleaved edge over growth, growth of vicinal substrates, strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum wells, semiconductor nanocrystals, collidal quantum dots, self-assembly techniques.

UNIT-IV

UNIT-V
Applications: Injectionlasers, quantumcascadelasers, singlephotonsources, biologicaltagging, optcialmemories, coulomb blockade devices, photonic structures, QWIP’s, NEMS, MEMS.
TEXT BOOKS

REFERENCE BOOKS
MTVL1061-MODERN DSP

Lecture : 4 Periods/week
Internal Marks : 40
External Marks : 60
Credits : 3
External Examination : 3 Hrs

UNIT-I
**Introduction and Discrete Fourier Transforms**: Signals, Systems and Processing, Classification of Signals, The Concept of Frequency in Continuous-Time and Discrete-Time Signals, Analog-to-Digital and Digital-to-Analog Conversion, Frequency-Domain Sampling: The Discrete Fourier Transform, Properties of the DFT, Linear Filtering Methods Based on the DFT (Ref.1 Chap. 1 & 7)

UNIT-II
**Design of Digital Filters**: General Considerations, Design of FIR Filters, Design of IIR Filters from Analog Filters, Frequency Transformations. (Ref.1 Chap.10)

UNIT-III
**Multirate Digital Signal Processing I**: Introduction, EL Dimation by a factor ‘D’, Interpolation by a factor ‘I’, Sampling rate Conversion by a factor ‘I/D’, implementation of Sampling rate conversion, Multistage implementation of Sampling rate conversion

UNIT-IV
**Multirate Digital Signal Processing II**: Sampling rate conversion of Band Pass Signals, Sampling rate conversion by an arbitrary factor, Applications of Multirate Signal Processing, Digital Filter banks, Two Channel Quadrature Mirror Filter banks, M-Channel QMF bank. (Ref.1 Chap.11)

UNIT-V
**Adaptive Filters**: Applications of Adaptive Filters, Adaptive Direct Form FIR Filters- The LMS Algorithm, Adaptive Direct Form Filters-RLS Algorithm. (Ref.1 Chap.13)

**TEXT BOOKS**

**REFERENCE BOOKS**
MTVL1062-EMBEDDED LINUX AND BASICS OF DEVICE DRIVERS

Lecture : 4 Periods/week
Credits : 3

Internal Marks : 40
External Marks : 60
External Examination : 3 Hrs

UNIT–I
**Introduction:** History of Embedded Linux, Embedded Linux versus Desktop Linux, Embedded Linux Distributions, Architecture of Embedded Linux, Linux Kernel Architecture, Linux Start-Up Sequence, GNU Cross-platform Tool chain.

UNIT–II
**Board Support Package:** Inserting BSP in Kernel Build Procedure, Boot Loader Interface, Memory Map, Interrupt Management, PCI Subsystem, Timers, UART, and Power Management.
**Embedded Storage:** Flash Map, MTD—Memory Technology Device, MTD Architecture, Flash-Mapping Drivers, MTD Block and Character devices, Embedded File systems, Optimizing Storage Space.

UNIT–III
**Embedded Drivers:** Linux Serial Driver, Ethernet Driver, I2C subsystem on Linux, USB Gadgets, Watchdog Timer, and Kernel Modules.

UNIT–IV
**Porting Applications:** Architectural Comparison, Application Porting Road Map, Programming with Pthreads, Operating System Porting Layer (OSPL), Kernel API Driver.

UNIT–V
**Real-Time Linux:** Linux and Real-Time, Real-Time Programming in Linux, Hard Real-Time Linux.

TEXT BOOK

REFERENCE BOOKS
1. Embedded Linux – Hardware, Software and Interfacing
MTVL1063-HIGH SPEED VLSI DESIGN

Lecture : 4 Periods/week  
Internal Marks : 40  
External Marks : 60  

Credits : 3  
External Examination : 3 Hrs

UNIT-I
Introduction to high speed digital design: Frequency, time and distance issues in digital VLSI design. Capacitance and inductance effects, high speed properties of logic gates, speed and power. Modeling of wires, geometry and electrical properties of wires, Electrical models of wires, transmission lines, lossless LC transmission lines, lossy RLC transmission lines and special transmission lines.

UNIT-II

UNIT-III
Signaling convention and circuits: Signaling modes for transmission lines, signaling over lumped transmission media, signaling over RC interconnect, driving lossy LC lines, simultaneous bi-directional signaling terminations, transmitter and receiver circuits.

UNIT-IV
Timing convention and synchronization: Timing fundamentals, timing properties of clocked storage elements, signals and events, open loop timing, level sensitive clocking, pipeline timing, closed loop timing, clock distribution, synchronization failure and metastability, clock distribution, clock skew and methods to reduce clock skew, controlling crosstalk in clock lines, delay adjustments, clock oscillators and clock jitter - PLL and DLL based clock aligners.

UNIT-V
Latching Strategies:
Basic Latch Design, and Latching single-ended logic and Differential Logic, Race Free Latches for Pre-charged Logic Asynchronous Latch Techniques

TEXT BOOKS

REFERENCE BOOKS
MTVL151-VLSI DESIGN LABORATORY

Practical : 3 Periods/week  Internal Marks : 25
Credits : 2  External Marks : 50
External Examination : 3 Hrs

Note:
- Minimum of 10 programs from Part –I and 2 programs from Part -II are to be conducted.
- Design and implementation of the following CMOS digital/analog circuits using Cadence / Mentor Graphics / Synopsys / Equivalent CAD tools. The design shall include Gate-level design, Transistor-level design, Hierarchical design, Verilog HDL/VHDL design, Logic synthesis, Simulation and verification.

Part –I: VLSI Front End Design programs:

Programming can be done using any complier. Down load the programs on FPGA/CPLD boards and performance testing may be done using pattern generator (32 channels) and logic analyzer apart from verification by simulation with any of the front end tools.

1. HDL code to realize all the logic gates
2. Design and Simulation of adder, Serial Binary Adder, Multi Precession Adder, Carry Look Ahead Adder.
3. Design of 2-to-4 decoder
4. Design of 8-to-3 encoder (without and with parity)
5. Design of 8-to-1 multiplexer
6. Design of 4 bit binary to gray converter
7. Design of Multiplexer/ Demultiplexer, comparator
8. Design of Full adder using 3 modeling styles
9. Design of flip flops: SR, D, JK, T
10. Design of 4-bit binary, BCD counters (synchronous/ asynchronous reset) or any sequence counter
12. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
13. Design of 4- Bit Multiplier, Divider.
14. Design of ALU to Perform – ADD, SUB, AND-OR, 1’s and 2’s Compliment, Multiplication, and Division.
15. Design of Finite State Machine.
16. Implementing the above designs on Xilinx/Altera/Cypress/equivalent based FPGA/CPLD kits.
Part -II: VLSI Back End Design programs:

- Design and implementation of the following CMOS digital/analog circuits using Cadence / Mentor Graphics / Synopsys / Equivalent CAD tools.

- The design shall include Gate-level design/Transistor level design/Hierarchical design/Verilog HDL or VHDL design. Logic synthesis, Simulation and verification, Scaling of CMOS Inverter for different technologies, study of secondary effects (temperature, power supply and process corners), Circuit optimization with respect to area, performance and/or power, Layout, Extraction of parasitics and back annotation, modifications in circuit parameters and layout consumption, DC/transient analysis, Verification of layouts (DRC, LVS).

1. Introduction to layout design rules

2. Layout, physical verification, placement & route for complex design, static timing analysis, IR drop analysis and crosstalk analysis of the following:
   - Basic logic gates
   - CMOS inverter
   - CMOS NOR/ NAND gates
   - CMOS XOR and MUX gates
   - CMOS 1-bit full adder
   - Static / Dynamic logic circuit (register cell)
   - Latch
   - Pass transistor

3. Layout of any combinational circuit (complex CMOS logic gate)- Learning ABOUT DATA PATHS
II SEMESTER
MTVL201-LOW POWER VLSI DESIGN

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UNIT-I
Introduction: Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches, Physics of power dissipation in CMOS devices.


UNIT-II
Power estimation, Simulation Power analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation.

Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

UNIT-III
Low Power Design Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library.
Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic.

UNIT- IV
Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.

Low power Clock Distribution: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network.

UNIT-V

TEXT BOOK

REFERENCE BOOKS

Department of Electronics & Communication Engineering
Lakireddy Bali Reddy College of Engineering
Mylavaram, Krishna Dt., Andhra Pradesh
MTVL202-DESIGN OF ANALOG AND MIXED MODE VLSI CIRCUITS

Lecture : 4 Periods/week
Credits : 3

Internal Marks : 40
External Marks : 60
External Examination : 3 Hrs

UNIT-I
Basic MOS Device Physics: General considerations, MOS I/V Characteristics, second order effects, MOS device models.
Single stage Amplifier: CS stage with resistance load, divide connected load, current source load, triode load, CS stage with source degeneration, source follower, common-gate stage, cascade stage, choice of device models.

UNIT-II
Frequency response of CS stage: source follower, Common gate stage, Cascade stage and Difference pair.Noise in CS stage, C- G stage, source follower, cascade stage, differential pair.
Differential Amplifiers & Current Mirrors: Basic difference pair, common mode response, Differential pair with MOS loads, Gilbert cell. Basic current mirrors, Cascade mirrors, active current mirrors.

UNIT-III
Oscillators and Phase Locked Loops: Ring Oscillators, LC Oscillators, VCO, Mathematical Model of VCO. Simple PLL, Charge pump PLL, Non-ideal effects in PLL, Delay locked loops and applications.

UNIT-IV
Bandgap References and Switched capacitor Circuits: General Considerations, Supply Independent biasing, PTAT Current Generation, Constant Gm Biasing, Sampling Switches, Switched Capacitor Amplifiers.

UNIT-V

TEXT BOOK
MTVL203-CRYPTOGRAPHY & NETWORK SECURITY

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UNIT-I


UNIT-II

Modern Techniques: Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations.


Conventional Encryption: Placement of Encryption function, Traffic confidentiality, Key distribution, Random Number Generation.


UNIT-III

Number theory: Prime and Relatively prime numbers, Modular arithmetic, Fermat’s and Euler’s theorems, Testing for primality, Euclid’s Algorithm, the Chinese remainder theorem, Discrete logarithms.

Message authentication and Hash functions: Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash Functions and MACs

UNIT-IV


UNIT-V


Web Security

TEXT BOOK

REFERENCES
1. Principles of Network and Systems Administration, Mark Burgess, John Wiel
MTVL204-ADVANCED EMBEDDED SYSTEMS

Lecture : 4 Periods/week  
Internal Marks : 40
External Marks : 60
Credits : 3  
External Examination : 3 Hrs

UNIT-I

**Typical Embedded System** : Core of the Embedded System, Memory, Sensors and Actuators, Communication Interface, Embedded Firmware, Other System Components.


UNIT-II

**Embedded Hardware Design and Development** : EDA Tools, How to Use EDA Tool, Schematic Design – Place wire, Bus, port, junction, creating part numbers, Design Rules check, Bill of materials, Netlist creation, PCB Layout Design – Building blocks, Component placement, PCB track routing.

UNIT-III


UNIT-IV

**Embedded Firmware Design and Development** : Embedded Firmware Design Approaches, Embedded Firmware Development Languages

**Real-Time Operating System (RTOS) based Embedded System Design** : Operating System Basics, Types of OS, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling, Threads, Processes and Scheduling: Putting them altogether, Task Communication, Task Synchronization, Device Drivers, How to Choose an RTOS

UNIT-V

**The Embedded System Development Environment** : The Integrated Development Environment (IDE), Types of Files Generated on Cross compilation, Disassembler /ELDmpiler, Simulators, Emulators and Debugging, Target Hardware Debugging, Boundary Scan.

TEXT BOOK


REFERENCE BOOKS

MTVL2051-SYSTEM MODELING AND SIMULATION

<table>
<thead>
<tr>
<th>Lecture</th>
<th>Internal Marks</th>
<th>Credits</th>
<th>External Examinetion</th>
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<td>4 Periods/week</td>
<td>40</td>
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UNIT-I

UNIT-II

UNIT-III

UNIT-IV
**System Optimization:** System Identification, Searches, Alpha / Beta trackers, Multidimensional Optimization, Modeling and Simulation Methodology.

UNIT-V
**Simulation Software and Building Simulation Models:**
Comparison of Simulation Packages with Programming Languages, Classification of Simulation Software, Desirable software features, General Purpose Simulation Packages-Arena, Extend; Guide lines for determining the level of Model detail, Techniques for increasing Model Viability and credibility.

TEXT BOOKS

REFERENCES
1. Systems Simulation-Geoffery Gordan, PHI.
MTVL2052-VLSI ARCHITECTURES FOR SIGNAL PROCESSING

Lecture : 4 Periods/week

Internal Marks : 40

External Marks : 60

Credits : 3

External Examination : 3 Hrs

UNIT-I
Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms

UNIT-II

UNIT-III

UNIT-IV

UNIT-V

TEXT BOOKS

REFERENCES
MTVL2053-DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES

Lecture : 4 Periods/week  
Internal Marks : 40  
External Marks : 60  
Credits : 3  
External Examination : 3 Hrs

UNIT-I
Computational Accuracy in DSP Implementations: Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT-II
Architectures for Programmable DSP Devices: Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT-III
Programmable Digital Signal Processors: Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

UNIT-IV
Introduction to Blackfin Processor – The Blackfin Processor, Introduction to Micro Signal Architecture, Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals.

UNIT-V
Interfacing Memory And I/O Peripherals To Programmable DSP Devices: Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

TEXT BOOKS
REFERENCES
4. Digital Signal Processing Applications Using the ADSP-2100 Family by The Applications Engineering Staff of Analog Devices, DSP Division, Edited by Amy Mar, PHI.
MTVL2061-INTERNET OF THINGS (IOT)

Lecture : 4 Periods/week
Credits   : 3

Internal Marks : 40
External Marks  : 60
External Examination : 3 Hrs

UNIT-I
The IoT Networking Core : Technologies involved in IoT Development: Internet/Web and Networking Basics OSI Model, Data transfer referred with OSI Model, IP Addressing, Point to Point Data transfer, Point to Multi Point Data transfer & Network Topologies, Sub-netting, Network Topologies referred with Web, Introduction to Web Servers, Introduction to Cloud Computing

UNIT-II

UNIT-III

UNIT-IV

UNIT-V

TEXT BOOKS
1. 6LoWPAN: The Wireless Embedded Internet, Zach Shelby, Carsten Bormann, Wiley
2. Internet of Things: Converging Technologies for Smart Environments and Integrated Ecosystems, Dr. OvidiuVermesan, Dr. Peter Friess, River Publishers

REFERENCES
1. The Internet of Things: From RFID to the Next-Generation Pervasive Networked Lu Yan, Yan Zhang, Laurence T. Yang, HuanshengNing
2. Internet of Things (A Hands-on-Approach), Vijay Madisetti, ArshdeepBahga
UNIT-I

UNIT-II

UNIT-III
Embedded Memories – cache memories, flash memories, embedded DRAM. Topics related to cache memories. Cache coherence. MESI protocol and Directory-based coherence.

UNIT-IV

UNIT-V
MPSoCs: What, Why, How MPSoCs, Techniques for designing MPSoCs, Performance and flexibility for MPSoCs design
Case Study: A Low Power Open Multimedia Application Platform for 3G Wireless.

TEXT BOOKS

REFERENCES
MTVL2063-VLSI TESTING AND VERIFICATION

Lecture : 4 Periods/week  
Internal Marks : 40  
External Marks : 60  
Credits : 3  
External Examination : 3 Hrs

UNIT-I
Test Generation for Combinational Logic Circuits: Fault Diagnosis of Digital Circuits, Test Generation Techniques for Combinational Circuits, Detection of Multiple Faults in Combinational Logic Circuits.

UNIT-II

UNIT-III
Testable Memory Design: RAM Fault Models, Test Algorithms for RAMs, Detection of Pattern Sensitive Faults, BIST Techniques for Ram Chips, Test Generation and BIST for Embedded RAMs.
Importance of Design Verification: What is verification? What is attest bench? The importance of verification, Reconvrence model, Formal verification, Equivalence checking, Model checking, Functional verification.[Ref4- Chapter1]

UNIT-IV
Verification Tools: Linting tools: Limitations of linting tools, lintingverilog source code, linting VHDL source code, lintingOpenVera and esourcecode, code reviews. Simulators: Stimulus and response, Event based simulation, cycle based simulation, Co-simulators, verification intellectual property: hardware modelers, waveform viewers.[Ref4-Chapter2]
The verification plan: The role of verification plan: specifying the verification plan, defining the first success. Levels of verification: unit level verification, reusable components verification, ASIC and FPGA verification, system level verification, board level verification, verifying strategies, verifying responses. [Ref4-Chapter3]

UNIT-V
Static Timing Verification: Concept of static timing analysis. Cross talk and noise. Limitations of STA. slew of a wave form, Skew between the signals, Timing arcs and unateness, Min and Max timing paths, clock domains, operating conditions, critical path analysis, falsepaths, Timing models. [Ref5 Chapter 1, 2, 3, 8]
Physical Design Verification: Layout rule checks and electrical rule checks. Parasitic extraction. Antenna, Crosstalk and Noise: Cross talk glitch analysis, crosstalk delay analysis, timing verification [Ref6 Chapter 8]
TEXT BOOKS

REFERENCES
MTVL251-EMBEDDED SYSTEMS LABORATORY

Practical : 3 Periods/week  
Internal Marks : 25
External Marks : 50
Credits : 2  
External Examination : 3 Hrs

Note:

The following programs are to be implemented on ARM based Processors/Equivalent. **Minimum of 5 programs from Part –I and 5 programs from Part –II are to be conducted.**

Part III programs are compulsory

Part-I

The following Programs are to be implemented on ARM Processor

1. Simple Assembly Program for
   a. Addition | Subtraction | Multiplication | Division
   b. Operating Modes, System Calls and Interrupts
   c. Loops, Branches
2. Write an Assembly programs to configure and control General Purpose Input/Output (GPIO) port pins.
3. Write an Assembly programs to read digital values from external peripherals and execute them with the Target board.
4. Program for reading and writing of a file
5. Program to demonstrate Time delay program using built in Timer / Counter feature on IDE environment
6. Program demonstrates setting up interrupt handlers. Press button to generate an interrupt and trace the program flow with debug terminal.
7. Program to Interface 8 Bit LED and Switch Interface
8. Program to implement Buzzer Interface on IDE environment
9. Program to Displaying a message in a 2 line x 16 Characters LCD display and verify the result in debug terminal.
10. Program to demonstrate I2C Interface on IDE environment
11. Demonstration of Serial communication. Transmission from Kit and reception from PC using Serial Port on IDE environment use debug terminal to trace the program.
12. Generation of PWM Signal

Part-II

Write the following programs to understand the use of RTOS with ARM Processor on IDE Environment using ARM Tool chain and Library:

1. Create an application that creates two tasks that wait on a timer whilst the main task loops.
2. Write an application that creates a task which is scheduled when a button is pressed, which illustrates the use of an event set between an ISR and a task
3. Write an application that Demonstrates the interruptible ISRs(Requires timer to have higher priority than external interrupt button)
4. a) Write an application to test message queues and memory blocks.
   b) Write an application to test byte queues
5. Write an application that creates two tasks of the same priority and sets the time slice period to illustrate time slicing.

   Interfacing Programs:
6. Write an application that creates a two task to Blinking two different LEDs at different timings
7. Write an application that creates a two task displaying two different messages in LCD display in two lines.
8. Sending messages to mailbox by one task and reading the message from mailbox by another task.
9. Sending message to PC through serial port by three different tasks on priority Basis.
10. Basic Audio Processing on IDE environment.

Part-III

The following programs are to be implemented on Xilinx FPGA Zynq 7000 series/Equivalent.
1. Design of System On Chip platform using Xilinx FPGAs and Embedded Development Kit Tools
2. Design dual processor based System on chip using Xilinx EDK Tools and Zynq 7000 series FPGA
3. Hardware Software co-design using Xilinx EDK Tools and Advanced FPGA Board Zynq 7000 series