LAKIREDDY BALIREDDY COLLEGE OF ENGINEERING (AUTONOMOUS)

(Approved by AICTE, Accredited by NBA,
Affiliated to JNTUK, Kakinada and ISO 9001: 2008 Certified)

ACADEMIC REGULATIONS,
COURSE STRUCTURE
AND
DETAILED SYLLABUS

2010 - 2011

M.TECH – SYSTEMS AND SIGNAL PROCESSING

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

L.B.Reddy Nagar, MYLAVARAM – 521 230
Krishna District, Andhra Pradesh State
## M.TECH(ECE – SYSTEMS AND SIGNAL PROCESSING) - COURSE STRUCTURE

### I-SEMESTER

<table>
<thead>
<tr>
<th>Code No.</th>
<th>Name of the Course</th>
<th>Scheme of Instruction</th>
<th>Scheme of Examination</th>
<th>Total</th>
<th>credits</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Periods per Week</td>
<td>Maximum Marks</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Lecture</td>
<td>Tutorial</td>
<td>Lab.</td>
<td>Internal</td>
</tr>
<tr>
<td>MEC101</td>
<td>Advanced Digital Signal Processing</td>
<td>4</td>
<td>-</td>
<td>-</td>
<td>40</td>
</tr>
<tr>
<td>MEC102</td>
<td>Transform Techniques</td>
<td>4</td>
<td>-</td>
<td>-</td>
<td>40</td>
</tr>
<tr>
<td>MEC103</td>
<td>VLSI Technology and Design</td>
<td>4</td>
<td>-</td>
<td>-</td>
<td>40</td>
</tr>
<tr>
<td>MEC104</td>
<td>Microcontrollers For Embedded System Design</td>
<td>4</td>
<td>-</td>
<td>-</td>
<td>40</td>
</tr>
<tr>
<td></td>
<td><strong>ELECTIVE – I</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEC1051</td>
<td>DSP Processors &amp; Architecture</td>
<td>4</td>
<td>-</td>
<td>-</td>
<td>40</td>
</tr>
<tr>
<td>MEC1052</td>
<td>Image and Video Processing</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td><strong>ELECTIVE – II</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEC1061</td>
<td>Radar Signal Processing</td>
<td>4</td>
<td>-</td>
<td>-</td>
<td>40</td>
</tr>
<tr>
<td>MEC1062</td>
<td>Bio – Medical Signal Processing</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEC151</td>
<td>Seminar</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>50</td>
</tr>
<tr>
<td>MEC152</td>
<td>Advanced Digital Signal Processing Lab</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>40</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td></td>
<td>24</td>
<td>-</td>
<td>6</td>
<td>330</td>
</tr>
</tbody>
</table>
### II-SEMESTER

<table>
<thead>
<tr>
<th>Code No.</th>
<th>Name of the Course</th>
<th>Scheme of Instruction</th>
<th>Scheme of Examination</th>
<th>Total</th>
<th>credits</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Periods per Week</td>
<td>Maximum Marks</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Lecture</td>
<td>Tutorial</td>
<td>Lab.</td>
<td>Internal</td>
</tr>
<tr>
<td>MEC201</td>
<td>Adaptive Signal Processing</td>
<td>4</td>
<td>--</td>
<td>--</td>
<td>40</td>
</tr>
<tr>
<td>MEC202</td>
<td>Speech Processing</td>
<td>4</td>
<td>--</td>
<td>--</td>
<td>40</td>
</tr>
<tr>
<td>MEC203</td>
<td>SOC Architecture</td>
<td>4</td>
<td>--</td>
<td>--</td>
<td>40</td>
</tr>
<tr>
<td>MEC204</td>
<td>Coding Theory and Techniques</td>
<td>4</td>
<td>--</td>
<td>--</td>
<td>40</td>
</tr>
<tr>
<td>ELECTIVE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEC2051</td>
<td>CPLD &amp; FPGA Architectures And Applications</td>
<td>4</td>
<td>--</td>
<td>--</td>
<td>40</td>
</tr>
<tr>
<td>MEC2052</td>
<td>Design for Testability</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ELECTIVE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEC2061</td>
<td>Wireless Communication and Networks</td>
<td>4</td>
<td>--</td>
<td>--</td>
<td>40</td>
</tr>
<tr>
<td>MEC2062</td>
<td>VLSI Signal Processing</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEC207</td>
<td>Seminar</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEC208</td>
<td>Advanced ECAD Lab</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TOTAL</td>
<td></td>
<td>24</td>
<td>--</td>
<td>6</td>
<td>330</td>
</tr>
</tbody>
</table>

### III & IV SEMESTERS

<table>
<thead>
<tr>
<th>Code No.</th>
<th>Name of the Course</th>
<th>Scheme of Instruction</th>
<th>Scheme of Examination</th>
<th>Total</th>
<th>credits</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Periods per Week</td>
<td>Maximum Marks</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Lecture</td>
<td>Tutorial</td>
<td>Lab.</td>
<td>Internal</td>
</tr>
<tr>
<td>MEC351</td>
<td>Technical Seminar</td>
<td>--</td>
<td>--</td>
<td>6</td>
<td>50</td>
</tr>
<tr>
<td>MEC451</td>
<td>Dissertation</td>
<td>--</td>
<td>--</td>
<td>15</td>
<td>50</td>
</tr>
<tr>
<td>TOTAL</td>
<td></td>
<td>--</td>
<td>--</td>
<td>21</td>
<td>100</td>
</tr>
</tbody>
</table>
I SEMESTER
MEC101: ADVANCED DIGITAL SIGNAL PROCESSING

Lecture : 4 Periods/week  
Internal Marks : 40  
External Marks : 60  
Credits : 4  
External Examination : 3 Hrs

UNIT - I

Review of DFT, FFT, IIR Filters, FIR Filters, Multirate Signal Processing: Introduction, Decimation by a factor D, Interpolation by a factor I, Sampling rate conversion by a rational factor I/D, Multistage Implementation of Sampling Rate Conversion, Filter design & Implementation for sampling rate conversion, Applications of Multirate Signal Processing

UNIT - II

Non-Parametric methods of Power Spectral Estimation: Estimation of spectra from finite duration observation of signals, Non-parametric Methods: Bartlett, Welch & Blackman & Tukey methods, Comparison of all Non-Parametric methods

UNIT - III


UNIT - IV

Linear Prediction: Forward and Backward Linear Prediction – Forward Linear Prediction, Backward Linear Prediction, Optimum reflection coefficients for the Lattice Forward and Backward Predictors. Solution of the Normal Equations: Levinson Durbin Algorithm, Schur Algorithm. Properties of Linear Prediction Filters

UNIT - V


TEXTBOOKS

2. Discrete Time signal processing -Alan V Oppenheim & Ronald W Schaffer, PHI.

REFERENCES:

MEC102: TRANSFORM TECHNIQUES

<table>
<thead>
<tr>
<th>Lecture</th>
<th>Internal Marks</th>
<th>4 Periods/week</th>
<th>40</th>
</tr>
</thead>
<tbody>
<tr>
<td>Credits</td>
<td>External Marks</td>
<td>60</td>
<td></td>
</tr>
<tr>
<td></td>
<td>External Examinatipn</td>
<td>3 Hrs</td>
<td></td>
</tr>
</tbody>
</table>

UNIT – I

Review of Transforms: Signal spaces, concept of convergence, Hilbert spaces for energy signals, Fourier basis, FT-failure of FT-need for time-frequency analysis, spectrogram plot-phase space plot in time-frequency plane, Continuous FT, DTFT, Discrete Fourier Series and Transforms, Z-Transform, relation between CFT-DTFT, DTFT-DFS,DFS-DFT, DCT(1D&2D), Walsh, Hadamard, Haar, Slant, KLT,Hilbert Transforms – definition, properties and applications

UNIT – II


UNIT – III

Multirate Systems, Filter Banks and DWT.
Basics of Decimation and Interpolation in time & frequency domains, Two-channel Filter bank, Perfect Reconstruction Condition, Relation ship between Filter Banks and Wavelet basis, DWT Filter Banks For Daubechies Wavelet Function

UNIT – IV

Special Topics: Wavelet Packet Transform Multidimensional Wavelets, Bi-orthogonal basis-B-splines, Lifting Scheme of Wavelet Generation, Multi Wavelets

UNIT – V

Applications of Transforms
Signal Denoising, Subband Coding of Speech and Music, Signal Compression - Use of DCT, DWT,KLT, 2-D DWT, Fractal Signal Analysis.

TEXT BOOKS

REFERENCES

MEC103: VLSI TECHNOLOGY AND DESIGN

Lecture : 4 Periods/week  
Internal Marks : 40  
External Marks : 60  
Credits : 4  
External Examination : 3 Hrs

UNIT - I

Review of Microelectronics and Introduction to MOS Technologies: MOS, CMOS, BiCMOS Technology, Trends And Projections. Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: \( I_d - V_d \) relationships, Threshold Voltage \( V_t \), \( G_m \), \( G_d \) and \( \omega_0 \), Pass Transistor, MOS, CMOS & Bi CMOS Inverters, \( Z_{pu}/Z_{pd} \), MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT - II


LOGIC GATES & LAYOUTS: Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT - III

COMBINATIONAL LOGIC NETWORKS: Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

UNIT - IV

SEQUENTIAL SYSTEMS: Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT – V

FLOOR PLANNING & ARCHITECTURE DESIGN: Floor planning methods, off-chip connections, High-level synthesis, Architecture for low power, SOCs and Embedded CPUs, Architecture testing.

TEXT BOOKS


REFERENCES

MEC104: MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN

Lecture : 4 Periods/week
Internal Marks : 40
External Marks : 60
Credits : 4
External Examination : 3 Hrs

UNIT – I


UNIT – II

Microcontrollers and Processor Architecture & Interfacing 8051 Architecture, Input/Output Ports and Circuits, External Memory, Counters and Timers, PIC Controllers. Interfacing Processor (8051, PIC), Memory Interfacing, I/O Devices, Memory Controller and Memory arbitration Schemes.

UNIT – III

Embedded RISC Processors & Embedded System-on Chip Processor PSOC (Programmable System-on-Chip) architectures, Continuous Timer blocks, Switched Capacitor blocks, I/O blocks, Digital blocks, Programming of PSOC, Embedded RISC Processor architecture – ARM Processor architecture, Register Set, Modes of operation and overview of Instructions

UNIT – IV

Interrupts & Device Drivers Exceptions and Interrupt handling Schemes – Context & Periods for Context Switching, Deadline & interrupt latency. Device driver using Interrupt Service Routine, Serial port Device Driver, Device drivers for Internal Programmable timing devices

UNIT – V

Network Protocols Serial communication protocols, Ethernet Protocol, SDMA, Channel & IDMA, External Bus Interface

TEXT BOOKS


REFERENCES

MEC1051: DIGITAL SIGNAL PROCESSORS AND ARCHITECTURE

Lecture : 4 Periods/week
Internal Marks : 40
External Marks : 60
Credits : 4
External Examination : 3 Hrs

UNIT - I

INTRODUCTION TO DIGITAL SIGNAL PROCESSING
Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation, Analysis and Design tool for DSP Systems MATLAB, DSP using MATLAB.

COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS
Number formats for signals and coefficients in DSP systems. Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT - II

ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES
Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT - III

EXECUTION CONTROL AND PIPELINING
Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.

PROGRAMMABLE DIGITAL SIGNAL PROCESSORS
Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

UNIT - IV

IMPLEMENTATIONS OF BASIC DSP ALGORITHMS
The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing.

IMPLEMENTATION OF FFT ALGORITHMS
An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.
UNIT - V

INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES
Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA). A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

TEXT BOOKS

REFERENCES

HEAD
Department of Electronics & Communication Engineering
Lakireddy Bali Reddy College of Engineering
Mylavaram Krishna Bt., Andhra Pradesh
MEC1052: IMAGE AND VIDEO PROCESSING

Lecture : 4 Periods/week
Internal Marks : 40
External Marks : 60
Credits : 4
External Examination : 3 Hrs

UNIT - I

Fundamentals of Image Processing and Image Transforms
Basic steps of Image Processing System Sampling and Quantization of an image – Basic relationship between pixels Image Transforms: 2-D Discrete Fourier Transform, Discrete Cosine Transform (DCT), Wavelet Transforms: Continuous Wavelet Transform, Discrete Wavelet Transforms.

UNIT - II

Image Processing Techniques – Image Enhancement Spatial domain methods:

Image Segmentation
Segmentation concepts, Point, Line and Edge Detection, Thresholding, Region Based segmentation.

UNIT - III

Image Compression
Image compression fundamentals - Coding Redundancy, Spatial and Temporal redundancy, Compression models: Lossy & Lossless, Huffman coding, Arithmetic coding, LZW coding, Run length coding, Bit plane coding, Transform coding, Predictive coding, Wavelet coding, JPEG Standards.

UNIT - IV

Basic steps of Video Processing

UNIT - V

2-D Motion Estimation
Optical flow, General Methodologies, Pixel Based Motion Estimation, Block-Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Region based Motion Estimation, Multi resolution motion estimation, Waveform based coding, Block based transform coding, Predictive coding, Application of motion estimation in Video coding.
TEXT BOOKS


REFERENCES

MEC1061: RADAR SIGNAL PROCESSING

Lecture : 4 Periods/week
Internal Marks : 40
External Marks : 60
Credits : 4
External Examination : 3 Hrs

UNIT - I


UNIT - II


UNIT - III


UNIT - IV


UNIT - V


TEXT BOOKS

REFERENCES

MEC1062: BIO-MEDICAL SIGNAL PROCESSING

| Lecture    | Internal Marks | 40
| External Marks | 60
| Credits | External Examination | 3 Hrs

UNIT - I


UNIT-II

Data Compression Techniques: Lossy and Lossless data reduction Algorithms. ECG data compression using Turning point, AZTEC, CORTES, Huffman coding, vector quantisation, DCTand the K L transform.

UNIT-III


UNIT-IV


UNIT-V


TEXT BOOKS

REFERENCES

MEC152: ADVANCED DIGITAL SIGNAL PROCESSING LAB

Lecture : 3 Periods/week

Internal Marks : 40

External Marks : 60

Credits : 2

External Examination : 3 Hrs

Cycle-1 SIGNALS & SYSTEM

1. Signal Classifications And Properties
2. Convolution
3. Correlation and Covariance of a Random Signal
4. Discrete Fourier Transform
5. Data Acquisition of Audio Signal using MATLAB

Cycle-2 FILTERS

6. Analog Filters
7. Digital Filters

Cycle-3 SPECTRAL ESTIMATION

8. Periodogram Based methods
9. Parametric Methods

Cycle-4 MULTIRATE SIGNAL PROCESSING

10. Decimation
11. Interpolation

Cycle-5 ADAPTIVE FILTERING

12. Least Mean Square Algorithm
13. Recursive Least Squares
14. Wiener Filter

Cycle-6 APPLICATIONS

15. Average Energy Calculation
16. Effect of Window Length
17. Voiced or Unvoiced Detection
18. Pitch calculation
19. Spectral Subtraction method for Speech enhancement
MEC201: ADAPTIVE SIGNAL PROCESSING

Lecture : 4 Periods/week  Internal Marks : 40
External Marks : 60

Credits : 4  External Examination : 3 Hrs

UNIT – I


UNIT – II

Development of Adaptive Filter Theory & Searching the Performance surface:

Searching the performance surface – Methods & Ideas of Gradient Search methods - Gradient Searching Algorithm & its Solution - Stability & Rate of convergence - Learning Curves.

UNIT - III

Steepest Descent Algorithms
Gradient Search by Newton’s Method, Method of Steepest Descent, Comparison of Learning Curves.

UNIT – IV

LMS Algorithm & Applications

UNIT – V

Kalman filtering:

TEXT BOOKS


REFERENCES

MEC202: SPEECH PROCESSING

Lecture : 4 Periods/week  
Internal Marks : 40  
External Marks : 60  
Credits : 4  
External Examination : 3 Hrs

UNIT - I


UNIT - II

Time Domain Models for Speech Processing
Introduction- Window considerations, Short time energy and average magnitude Short time average zero crossing rate ,Speech vs. silence discrimination using energy and zero crossing, Pitch period estimation using a parallel processing approach, The short time autocorrelation function, The short time average magnitude difference function, Pitch period estimation using the autocorrelation function.

UNIT – III

Linear predictive coding (LPC) analysis

Homomorphic Speech Processing

UNIT - IV


Automatic speech recognition-Basic pattern recognition approaches, Parametric representation of speech, Evaluating the similarity of speech patterns, Isolated digit Recognition System, Continuous digit Recognition System

UNIT - V

Hidden Markov Model (HMM) for Speech
Hidden markov model (HMM) for speech recognition, Viterbialgorithm, Training and testing using HMMs,Adapting to variability in speech(DTW), Language models.
Speaker recognition
Recognition techniques, Features that distinguish speakers, Speaker Recognition Systems: Speaker Verification System, Speaker Identification System.

TEXT BOOKS

1. Digital processing of speech signals - L.R Rabiner and S.W.Schafer. Pearson Education.
3. Digital processing of speech signals. L.R Rabinar and R W Schafer, 1978, PHI.

REFERENCES


*****

HEAD
Department of Electronics & Communication Engineering
Lakireddy Bali Reddy College of Engineering
MYLAVARAM, Krishna Dt., Andhra Pradesh.
MEC203: SOC ARCHITECTURE

Lecture : 4 Periods/week
Internal Marks : 40

Credits : 4
External Marks : 60

External Examination : 3 Hrs

UNIT - I

Introduction to Processor Design:
Abstraction in Hardware Design, MUO a simple processor, Processor design trade off, Design for low power consumption.


UNIT - II

ARM Assembly Language Programming:
ARM instruction types – data transfer, data processing and control flow instructions – ARM instruction set – Co-processor instructions.


UNIT - III

Memory Hierarchy: Memory size and speed – On-chip memory – Caches – Cache design– an example – memory management

UNIT - IV


UNIT - V


HEAD
Department of Electronics &
Communication Engineering
Lakireddy Bali Reddy College of Engineering
Mylavaram, Krishna Dt., Andhra Pradesh

M.TECH (SYSTEMS AND SIGNAL PROCESSING), A.Y.2010-2011
TEXT BOOKS


REFERENCES

MEC204: CODING THEORY AND TECHNIQUES

<table>
<thead>
<tr>
<th>Lecture</th>
<th>: 4 Periods/week</th>
<th>Internal Marks</th>
<th>: 40</th>
</tr>
</thead>
<tbody>
<tr>
<td>Credits</td>
<td>: 4</td>
<td>External Marks</td>
<td>: 60</td>
</tr>
<tr>
<td></td>
<td></td>
<td>External Examination</td>
<td>: 3 Hrs</td>
</tr>
</tbody>
</table>

UNIT - I

Coding for Reliable Digital Transmission and storage: Mathematical model of Information, A Logarithmic Measure of Information, Average and Mutual Information and Entropy, Types of Errors, Error Control Strategies. Linear Block Codes: Introduction to Linear Block Codes, Syndrome and Error Detection, Minimum Distance of a Block code, Error-Detecting and Error-correcting Capabilities of a Block code, Standard array and Syndrome Decoding, Probability of an undetected error for Linear Codes over a BSC, Hamming Codes. Applications of Block codes for Error control in data storage system.

UNIT- II

Cyclic codes: Description, Generator and Parity-check Matrices, Encoding, Syndrome Computation and Error Detection, Decoding, Cyclic Hamming Codes, Shortened cyclic codes, Error-trapping decoding for cyclic codes, Majority logic decoding for cyclic codes.

UNIT- III

Convolutional codes: Encoding of Convolutional Codes, Structural and Distance Properties, maximum likelihood decoding, Sequential decoding, Majority- logic decoding of Convolutional codes. Application of Viterbi Decoding and Sequential Decoding, Applications of Convolutional codes in ARQ system.

UNIT- IV


UNIT – V

BCH – Codes: BCH code- Definition, Minimum distance and BCH Bounds, Decoding Procedure for BCH Codes- Syndrome Computation and Iterative Algorithms, Error Location Polynomials and Numbers for single and double error correction.

TEXT BOOKS

REFERENCES

1. Digital Communications-Fundamental and Application - Bernard Sklar, PE.
3. Introduction to Error Control Codes-Salvatore Gravano-oxford
MEC2051: CPLD & FPGA Architectures and Applications

Lecture: 4 Periods/week

Internal Marks: 40

External Marks: 60

Credits: 4

External Examination: 3 Hrs

UNIT - I

Programmable logic: ROM, PLA, PAL PLD, PGA – Features, programming and applications using complex programmable logic devices Altera series – Max 5000/7000 series and Altera FLEX logic-10000 series CPLD, AMD’s- CPLD (Mach 1 to 5), Cypres FLASH 370 Device technology, Lattice PLST’s architectures – 3000 series – Speed performance and in system programmability.

UNIT - II

FPGAs: Field Programmable gate arrays- Logic blocks, routing architecture, design flow technology mapping jfor FPGAs, Case studies Xitir x XC4000 & ALTERA’s FLEX 8000/10000 FPGAs: AT &T ORCA’s (Optimized Reconfigurable Cell Array): ACTEL’s ACT-1,2,3 and their speed performance

UNIT - III

Alternative realization for state machine using microprogramming linked state machine one –hot state machine, petrinet for state machines-basic concepts, properties, extended petrinets for parallel controllers.

UNIT - IV

Digital front end digital design tools for FPGAs& ASICs: Using mentor graphics EDA tool (“FPGA Advantage”) – Design flow using FPGAs

UNIT - V

Case studies of paraller adder cell paraller adder sequential circuits, counters, multiplexers, paraller controllers.

TEXT BOOKS


2. Field Programmable Gate Arrays, John V.Oldfield, Richard C Dore, Wiley Publications.
REFERENCES

MEC2052 : DESIGN FOR TESTABILITY

<table>
<thead>
<tr>
<th>Lecture</th>
<th>Internal Marks</th>
<th>External Marks</th>
<th>Credits</th>
<th>External Examination</th>
</tr>
</thead>
<tbody>
<tr>
<td>4 Periods/week</td>
<td>40</td>
<td>60</td>
<td>4</td>
<td>3 Hrs</td>
</tr>
</tbody>
</table>

**UNIT – I**

Introduction to Test and Design for Testability (DFT) Fundamentals

**UNIT – II**


**UNIT – III**


**UNIT – IV**

Design for Testability – testability Trade-off’s Techniques, Scan Architectures and Testing, Controllability and Absorbability, Generic Boundary Scan, Full Integrated Scan, Storage Cells for Scan Design, Board level and System level approaches, Boundary Scans Standards, Compression Techniques – Different Techniques, Syndrome test and Signature analysis.

**UNIT – V**


**TEXT BOOKS**

2. Design for Test for Digital ICs & Embedded Core Systems – Alfred Crouch, 2008, PE.

**REFERENCES**

MEC2061 : WIRELESS COMMUNICATION AND NETWORKS

Lecture : 4 Periods/week  Internal Marks : 40
External Marks : 60
Credits : 4  External Examination : 3 Hrs

UNIT - I

Wireless Communications & System Fundamentals: Introduction to wireless communications systems, examples, comparisons & trends. Cellular concepts—frequency reuse, strategies, interference & system capacity, trucking & grade of service, improving coverage & capacity in cellular systems.

UNIT - II

Multiple Access Techniques for Wireless Communication: FDMA, TDMA, SSMA (FHMA/CDMA/Hybrid techniques), SDMA technique (AS applicable to wireless communications). Packet radio access-protocols, CSMA protocols, reservation protocols, capture effect in packet radio, capacity of cellular systems.

UNIT - III


UNIT - IV

Mobile IP and Wireless Application Protocol: Mobile IP Operation of mobile IP, Co-located address, Registration, Tunneling, WAP Architecture, overview, WML scripts, WAP service, WAP session protocol, wireless transaction, Wireless datagram protocol. Wireless LAN Technology, Infrared LANs, Spread spectrum LANs, Narrow bank microwave LANs, IEEE 802 protocol Architecture, IEEE802 architecture and services, 802.11 medium access control, 802.11 physical layer.

UNIT - V


TEXT BOOKS


HEAD
Department of Electronics & Communication Engineering
Lakireddy Bali Reddy College of Engineering
Mylavaram Magathan Blt., Andhrapradesh

M.TECH (SYSTEMS AND SIGNAL PROCESSING), A.Y.2010-2011
REFERENCES

1. Wireless Digital Communications – Kamilo Feher, 1999, PHI.

MEC2062 : VLSI SIGNAL PROCESSING

<table>
<thead>
<tr>
<th></th>
<th>Lecture</th>
<th>Internal Marks</th>
<th>40</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>External Marks</td>
<td>60</td>
<td></td>
</tr>
<tr>
<td>Credits</td>
<td>External Examination</td>
<td>3 Hrs</td>
<td></td>
</tr>
</tbody>
</table>

**UNIT - I**

**Introduction to DSP:** Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms **Pipelining and Parallel Processing:** Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power **Retiming:** Introduction – Definitions and Properties – Solving System of Inequalities – Retiming Techniques

**UNIT - II**

**Folding and Unfolding:** Folding : Introduction -Folding Transform - Register minimization Techniques – Register minimization in folded architectures – folding of multirate systems **Unfolding:** Introduction – An Algorithm for Unfolding – Properties of Unfolding – critical Path, Unfolding and Retiming – Applications of Unfolding

**UNIT - III**

**Systolic Architecture Design:** Introduction – Systolic Array Design Methodology – FIR Systolic Arrays – Selection of Scheduling Vector – Matrix Multiplication and 2D Systolic Array Design – Systolic Design for Space Representations contain Delays

**UNIT – IV**

**Fast Convolution:** Introduction – Cook-Toom Algorithm – Winograd algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

**UNIT – V**


**TEXT BOOKS**


**REFERENCES**

MEC208: ADVANCED ECAD LAB

Lecture : 3 Periods/week
Internal Marks : 40
External Marks : 60
Credits : 2
External Examination : 3 Hrs

LIST OF EXPERIMENTS

Design FULL ADDER using verilog HDL and implementation on Sparten3E

1. FULL ADDER
2. MULTIPLEXER
3. PARALLEL ADDER
4. Combinational Multiplier
5. ALU
6. Counter
7. Linear feedback Shift Register
8. Decade Counter
9. 3-STAGE Decade Counter
10. Binary Multiplier
11. Digital Clock
12. DICE GAME

HEAD
Department of Electronics & Communication Engineering
Lakireddy Bali Reddy College of Engineering
Mylavaram, Kurnool, Andhra Pradesh