Digital System Design Lab

This lab is offered to B. Tech. ECE students, and it is specially designed and developed for modelling of combinational and sequential logic circuits using VHDL/Verilog and implementation of digital circuits on Xilinx FPGAs, In addition modelling of CMOS logic circuits using Mentor Graphics tool with complete ASIC flow. This lab is well provided with equipment Xilinx ISE System Edition 14.7, advanced Zynq-Zed development boards, Zynq-Zybo Z20 Deployment boards. This lab gives practical observation on design of CMOS logic gates using Pyxis Schematic Editor and digital system implemented on advanced Zynq boards. At the end of the semester the student will be able to Design CMOS Logic circuit modeling using pyxis schematic editor, Digital system modelling using VHDL and implementation on advanced Zynq boards. The Budget of this lab is around Rs. 15, 25, 000/-



Major Equipment:

S.No.	Name of the Equipment	Qty.	Cost in Rs.
1	HP desktop-intel(R) COR(TM) i3-3240 CPU @3.09GHZ,18.5'' LED	36	3,50,000.00
2	Xilinx ISE System Edition 14.7	25	1,17,747.00
3	XUP SPARTAN 3E Kit with USB Programming cable	5	1,20,000.00
4	Zynq-Zed development Board	4	1,72,661.00
5	Zynq-Zybo Z20 Deployment Board	6	1,74,000.00
6	Mentor Graphics complete ASIC tool and Tessent DFT tool	35 Users	5,30,930.00
7	APC 3 KV online UPS 6-UPS Batteries 26ah Exide 1-UPS Rack	01	61,000.00
	Total (Fifteen Lacks twenty six thousand Three hundred and thirty eight Rupees only)		**15,26,338.00**

List of Experiments (As per R14 Regulation):

S. No.	Name of the Experiment
1	Design CMOS Inverter
2	Design NAND and EX-OR gate
3	Design NOR and Ex-NOR gate
4	Design Adder and Implement on FPGA
5	Design 3X8 Decoder and Implement on FPGA
6	Design 4-BIT Magnitude Comparator and Implement
7	Design 8X1 Multiplexer, 1X4 De-multiplexer and Implement.
8	Design ALU and Implement.
9	Design Decade Counter and Implement.
10	Design UP/DOWN Counter and Implement.
11	Design Mealy Machine Modelling and Implement.
12	Design Moore's Machine Modelling and Implement.

List of Experiments (As per R17 Regulation):

S.No.	Name of the Experiment
1	Implementation of Logic Gates – Data flow model and Behavioral model
2	Combinational logic circuits – Adders and Subtractor
3	Code converters- Binary to Gray and Gray to Binary
4	3 to 8 Decoder – 74138.
5	4 Bit Comparator – 7485.
6	8 x 1 Multiplexer – 74151 and 2X4 De-multiplexer – 74155
7	16 x 1 Multiplexer – 74150 and 4X16 De-multiplexer – 74154
8	Sequential circuits - Flip-Flops
9	Decade counter – 7490.
10	Synchronous & Asynchronous Counters
11	Shift registers – 7495.
12	Universal shift registers – 74194/195.
13	RAM (16 x 4) – 74189 (Read and Write operations).
14	Stack and Queue Implementation using RAM.

List of Experiments (Beyond the Syllabus):

S.No.	Name of the Experiment
1	Design Stepper motor/LCD Controller and Implement
2	Design Flip Flops (JK, D, T) and Implement.
3	Design Shift Register and Implement.

Lab Mentor : Dr.G.Srinivasulu, Professor
Lab In-charge : Mr.G.Venkata Rao, Associate Professor
Lab Co-In-charge : Mr.K.V.Ashok, Assistant Professor
Lab Instructor : Mr. T.Prasad