M.Tech., R17 Course Structure (Choice Based Credit System)

I SEMESTER

S. No	Course Code	Course Title	Contact hours/week				Credits	Scheme of Valuation		
			L	T	P	Total		CIE	SEE	Total
1	17VE01	Digital VLSI System Design	3	-	-	3	3	40	60	100
2	17VE02	Embedded System Design	3	-	-	3	3	40	60	100
3	17VE03	CPLD and FPGA Architectures and Applications	3	-	-	3	3	40	60	100
4	PE-I	Programme Elective - I	3	-	-	3	3	40	60	100
5	PE-II	Programme Elective - II	3	-	-	3	3	40	60	100
6	17VE60	Digital VLSI System Design Lab	-	-	2	2	1	40	60	100
7	17VE61	Embedded System Design Lab	-	-	2	2	1	40	60	100
8	17VE50	Technical Seminar	-	-	2	2	1	100	--	100
10	17VE90	Advanced Computer Architecture	3	-	-	3	3	40	60	100
		Total	**15/ 18***	**-**	**6**	**21/ 24***	**18/ 21***	**380/ 420***	**420/ 480***	**800/ 900***

*With inclusion of Add on course

II SEMESTER

S. No	Course Code	Course Title	Contact hours/week				Credits	Scheme of Valuation		
			L	T	P	Total		CIE	SEE	Total
1	17VE10	Analog VLSI Design	3	-	-	3	3	40	60	100
2	17VE11	Real Time Operating Systems	3	-	-	3	3	40	60	100
3	17VE12	DSP Processors and Architecture	3	-	-	3	3	40	60	100
4	PE-III	Programme Elective -III	3	-	-	3	3	40	60	100
5	PE-IV	Programme Elective -IV	3	-	-	3	3	40	60	100
6	17VE62	Analog VLSI Design Lab	-	-	2	2	1	40	60	100
7	17VE63	Real Time Operating Systems Lab	-	-	2	2	1	40	60	100
8	17VE51	Mini Project	-	-	2	2	1	100	--	100
10	17VE91	ASIC Design	3	-	-	3	3	40	60	100
		Total	**15/ 18***	**-**	**6**	**21/ 24***	**18/ 21***	**380/ 420***	**420/ 480***	**800/ 900***

*With inclusion of Add on course

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III SEMESTER

S. No	Course Code	Course Title	Contact hours/week				Credits	Scheme of Valuation		
			L	T	P	Total		CIE	SEE	Total
1	PE-V	Programme Elective -V	3	-	-	3	3	40	60	100
2	PE-VI	Programme Elective-VI	3	-	-	3	3	40	60	100
3	17VE52	Internship	-	-	-	-	2	100	--	100
4	17VE53	Project Work (Phase-I)	-	-	20	20	10	40	60	100
		Total	**6**	**-**	**20**	**26**	**12/15/18**	**220**	**180**	**400**

IV SEMESTER

S. No	Course Code	Course Title	Contact hours/week				Credits	Scheme of Valuation		
			L	T	P	Total		CIE	SEE	Total
1	17VE54	Project Work (Phase-II)	-	-	32	32	16	40	60	100
2	17VE55	Comprehensive Viva Voce	-	-	4	4	2	100	--	100
		Total	**-**	**-**	**36**	**36**	**18**	**140**	**60**	**200**

List of courses for Programme Elective- I & II

S.No	CourseCode	Course Title
1	17VE04	Cryptography and Network Security
2	17VE05	Design for Internet of Things
3	17VE06	High Speed VLSI Design
4	17VE07	Image and Video Processing
5	17VE08	System Modeling and Simulation
6	17VE09	VLSI Design Automation

Note: Students are required to choose any two courses as Programme Elective- I & II

List of courses for Programme Elective- III& IV

S.No	Course Code	Course Title
1	17VE13	CMOS RF Circuit Design
2	17VE14	Embedded Software Design
3	17VE15	VLSI Testing and Verification
4	17VE16	VLSI Architecture for Signal Processing
5	17VE17	SOC Design
6	17VE18	Wireless Communications & Networks

Note: Students are required to choose any two courses as Programme Elective- III & IV.

List of courses for Programme Elective- V & VI

S.No	CourseCode	Course Title
1	17VE19	Design of Semiconductor Memories
2	17VE20	Embedded Linux
3	17VE21	Multimedia systems
4	17VE22	MEMS Design and Fabrication
5	17VE23	Nano Electronics
6	17VE24	Low Power VLSI Design

Note: Students are required to choose two/one courses as Programme Elective- III & IV, depending on the add-on-courses opted in Semester I & II.

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M.Tech. (I Sem.) **17VE01 - DIGITAL VLSI SYSTEM DESIGN**

L	T	P	Cr.
3	-	-	3

Pre-Requisites: STLD, CO

COURSE EDUCATIONAL OBJECTIVES:
In this course student will learn about the design of various combinational and sequential circuits using verilog HDL and VHDL, write the verilog tasks, functions, and various digital modules.

COURSE OUTCOMES: At the end of this course student will be able to
CO1 Design Combinational and Sequential circuits.
CO2 Understand Digital System Design flow using Verilog HDL.
CO3 Model Digital System Using Verilog HDL.
CO4 Write Verilog Tasks, Functions, UDPs for Digital modules.

UNIT-I: REVIEW OF LOGIC DESIGN FUNDAMENTALS.
MOS Devices and CMOS Logic. Combinational Logic. Boolean Algebra and Algebraic Simplification. Karnaugh Maps. Designing with NAND and NOR Gates. Hazards in Combinational Circuits. Flip-Flops and Latches. Mealy Sequential Circuit Design. Design of a Moore Sequential Circuit. Equivalent States and Reduction of State Tables. Sequential Circuit Timing. Tristate Logic and Busses.

UNIT-II: INTRODUCTION TO VERILOG.
Computer-Aided Design. Hardware Description Languages. Verilog Description of Combinational Circuits. Verilog Modules. Verilog Assignments. Procedural Assignments. Modeling Flip-Flops Using Always Block. Always Blocks Using Event Control Statements. Delays in Verilog. Compilation, Simulation, and Synthesis of Verilog Code. Verilog Data Types and Operators. Simple Synthesis Examples. Verilog Models for Multiplexers. Modeling Registers and Counters Using Verilog Always Statements. Behavioral and Structural Verilog. Constants. Arrays. Loops in Verilog. Testing Verilog Model. A Few Things to Remember.

UNIT-III: DESIGN EXAMPLES.
BCD to 7-Segment Display Decoder. A BCD Adder.32-Bit Adders. Traffic Light Controller. State Graphs for Control Circuits. Scoreboard and Controller. Synchronization and Debouncing. A Shift-and-Add Multiplier. Array Multiplier. A Signed Integer/Fraction Multiplier. Keypad Scanner. Binary Dividers.

UNIT-IV: SM CHARTS AND MIRCOPROGRAMMING.
State Machine Charts. Derivation of SM Charts. Realization of SM Charts. Implementation of the Dice Game. Microprogramming. Linked State Machines.

UNIT-V:ADDITIONAL TOPICS IN VERILOG & DESIGN OF A RISCMICROPROCESSOR
Verilog Functions. Verilog Tasks. Multi-Valued Logic and Signal Resolution. Built-in Primitives. User Defined Primitives. SRAM Model. Model for SRAM Read/Write System. Rise and Fall Delays of Gates. Named Association. Generate Statements. System Functions. Compiler Directives. File I/O Functions. Timing Check. The RISC Philosophy. The MIPS ISA. MIPS Instruction Encoding. Implementation of a MIPS Subset. VHDL Model.

TEXT BOOK
Digital Systems Design using VERILOG Charles H. Roth, Lizykurian John

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REFERENCES

1. Principles of CMOS VLSI Design – N.H.E. Weste, K. Eshraghian, 2nd Ed., Adisson Wesley.
2. CMOS VLSI Design A Circuits and Systems perspective Third Edition, NeilH.E. Weste.
3. Introduction to VLSI Systems – A Logic, Circuit and System Perspective – Ming Bo, Liu, CRC Press, 1st Edition, 2011.

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M.Tech. (I Sem.) **17VE02 - EMBEDDED SYSTEM DESIGN**

L	T	P	Cr.
3	-	-	3

Pre-Requisites: Computer Organization, Microprocessors and Microcontrollers

COURSE EDUCATIONAL OBJECTIVES:

In this course student will learn about the design methodologies of embedded systems, design the control unit and data-path unit for a given embedded system, interface between ARM processor, memory and co-processor etc.

COURSE OUTCOMES: At the end of this course student will be able to

CO1 Choose different design methodologies to implement given specifications.
CO2 Design control unit and Data path unit for given Embedded System.
CO3 Use ARM processor architecture for development of Embedded System.
CO4 Develop interface between ARM processor core, memory and co-processor.
CO5 Build frame work for embedded system using IC & design technology.

UNIT-I: Embedded System Introduction: Embedded systems overview, design challenge, processor technology, IC technology, Design Technology, Trade-offs. Single purpose processors RT-level combinational logic, sequential logic(RT level), custom single purpose processor design(RT –level), optimizing custom single purpose processors.

UNIT-II: State Machine and Concurrent Process Models: Introduction, models Vs languages, finite state machines with data path model(FSMD), using state machines, program state machine model (PSM), concurrent process model, concurrent process model, concurrent processes, communication among processes, synchronization among processes, Implementation, data flow model, real-time systems.

UNIT-III: ARM Processor Architecture: The ARM programmer's model, ARM development tools, ARM Assembly Language Programming: Data processing instructions, Data transfer instructions, Control flow instructions, writing simple assembly language programs,

UNIT-IV:ARM Organization and Implementation: 3-stage pipeline ARM organization, 5-stage pipeline ARM organization, ARM instruction execution, ARM implementation, The ARM coprocessor interface, The ARM memory interface, The ARM Instruction Set, The Thumb Instruction Set, ARM Processor Core ARM7TDMI

UNIT-V: IC and Design Technology: IC Technology: Full-Custom(VLSI) IC Technology, Semicustom(ASIC) IC Technology, Programmable logic device(PLD) IC technology, Design technology: automation: synthesis, verification: Hardware/Software Co-Simulation, Reuse: Intellectual Property cores, Design Process Models

TEXT BOOKS

1. "Embedded System Design A unified Hardware/Software Introduction" Frank Vahid/ Tony Givargis, John Wiley & Sons Pte Ltd.
2. "ARM System-On-Chip Architecture", 2nd Edition, Steve furber, Addison Wesley

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REFERENCES

1. Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education Private Limited, 2009
2. James K Peckol, "Embedded Systems – A Contemporary Design Tool", John Weily, 2008.
3. Joseph Yiu, "The Definitive Guide to the ARM Cortex-M3", Newnes, (Elsevier), 2008

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M.Tech. (I Sem.)	17VE03 - CPLD AND FPGA ARCHITECTURES AND APPLICATIONS	L	T	P	Cr.
		3	-	-	3

Pre-Requisites: Basics on CPLD and FPGA

COURSE EDUCATIONAL OBJECTIVES:

In this course student will learn about the complex programmable logic devices, field programmable gate arrays, architecture of SRAM programmable and anti-fuse programmed FPGAs.

COURSE OUTCOMES: At the end of this course student will be able to

CO1 **Analyze** different types of Complex Programmable Logic Devices.
CO2 **Understand** different types of Field Programmable Gate Arrays.
CO3 **Evaluate** architecture of SRAM Programmable FPGAs.
CO4 **Explain** the device Architecture of Anti-Fuse Programmed FPGAs.
CO5 **Design** the application for Combinational and Sequential Circuits.

UNIT - I

Introduction to Programmable Logic Devices:

Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic. Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD Implementation of a Parallel Adder with Accumulation.

UNIT – II

Field Programmable Gate Arrays:

Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects and Programmable I/O blocks in FPGAs, Dedicated specialized Components of FPGAs, Design flow and applications of FPGAs.

UNIT – III

SRAM Programmable FPGAs:

Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000, XC4000 Architectures.

UNIT – IV

Anti-Fuse Programmed FPGAs:

Introduction, Programming Technology, Device Architecture, TheActel ACT1, ACT2 and ACT3 Architectures.

UNIT – V

Design Applications:

General Design Issues, Counter Examples, A Fast Video Controller, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

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TEXTBOOKS

1. Field Programmable Gate Array Technology by Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design by Charles H. Roth Jr, LizyKurian John, Cengage Learning.

REFERENCES

1. Field Programmable Gate Arrays by John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays by Pak K. Chan/SamihaMourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs by Ian Grout, Elsevier, Newnes.
4. FPGA based System Design by Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

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M.Tech. (I Sem.)	17VE04 - CRYPTOGRAPHY AND NETWORK SECURITY	L	T	P	Cr.
		3	-	-	3

Pre-Requisites: Computer Networks

COURSE EDUCATIONAL OBJECTIVES:

In this course student will learn about the various security attacks and their characteristics, analyze the cryptographic techniques, concepts of digital signatures and its applications.

COURSE OUTCOMES: At the end of this course student will be able to

CO1 Discuss various types of attacks and their characteristics..
CO2 Analyze various cryptographic techniques.
CO3 Design public key cryptographic algorithms using the concepts from number theory.
CO4 Describe the concept of digital signature and its applications.
CO5 Illustrate the concepts of IP and Web security.

UNIT-I

Introduction: Attacks, Services and Mechanisms, Security attacks, Security services, A Model for Internetwork security. Classical Techniques: Conventional Encryption model, Steganography, Classical Encryption Techniques.

UNIT-II

Modern Techniques: Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations.

Algorithms: Triple DES, International Data Encryption algorithm, Blowfish, RC5, CAST-128, RC2, Characteristics of Advanced Symmetric block cifers.

Conventional Encryption: Placement of Encryption function, Traffic confidentiality, Key distribution, Random Number Generation.

Public Key Cryptography: Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange, Elliptic Curve Cryptography.

UNIT-III

Number theory: Prime and Relatively prime numbers, Modular arithmetic, Fermat's and Euler's theorems, Testing for primality, Euclid's Algorithm, the Chinese remainder theorem, Discrete logarithms.

Message authentication and Hash functions: Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash Functions and MACs

UNIT-IV

Hash and Mac Algorithms: MD File, Message digest Algorithm, Secure Hash Algorithm, RIPEMD-160, and HMAC. **Digital signatures and Authentication protocols**: Digital signatures, Authentication Protocols, Digital signature standards. **Authentication Applications**: Kerberos, X.509 directory Authentication service. Electronic Mail Security: Pretty Good Privacy, S/MIME.

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UNIT-V

IP Security: Overview, Architecture, Authentication, Encapsulating Security Payload, Combining security Associations, Key Management

Web Security

Web Security requirements, Secure sockets layer and Transport layer security, Secure Electronic Transaction. **Intruders, Viruses and Worms:**Intruders, Viruses and Related threats. **Fire Walls** Fire wall Design Principles, Trusted systems.

TEXT BOOK

Cryptography and Network Security: Principles and Practice - William Stallings, 2000, PE.

REFERENCE

Principles of Network and Systems Administration, Mark Burgess,JohnWiel

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M.Tech. (I Sem.) **17VE05 - DESIGN FOR INTERNET OF THINGS**

L	T	P	Cr.
3	-	-	3

Pre-Requisites: Networking Knowledge

COURSE EDUCATIONAL OBJECTIVES:

In this course student will learn about the Technologies used in IoT, build platform for various IoTs, analyzing the IoT architecture, performance and security aspects.

COURSE OUTCOMES: At the end of this course student will be able to

CO1 Understand technologies involved in IoT Development.
CO2 Build IoT platform using Raspberry pi, ARM and Arduino.
CO3 Analyze IoT architecture for performance and security aspects.
CO4 Develop IoT application using various protocols.
CO5 IntegrateBig Data and Visualization issues in IoT .

UNIT-I

The IoT Networking Core : Technologies involved in IoT Development: Internet/Web and Networking Basics OSI Model, Data transfer referred with OSI Model, IP Addressing, Point to Point Data transfer, Point to Multi Point Data transfer & Network Topologies, Sub-netting, Network Topologies referred with Web, Introduction to Web Servers, Introduction to Cloud Computing

UNIT-II

IoT Platform overview Overview of IoT supported Hardware platforms such as: Raspberry pi, ARM Cortex Processors, Arduino and Intel Galileo boards. Network Fundamentals: Overview and working principle of Wired Networking equipment's – Router, Switches, Overview and working principle of Wireless Networking equipment's – Access Points, Hubs etc. Linux Network configuration Concepts: Networking configurations in Linux Accessing Hardware & Device Files interactions.

UNIT-III

IoT Architecture: History of IoT, M2M – Machine to Machine, Web of Things, IoT protocols Applications: Remote Monitoring & Sensing, Remote Controlling,Performance Analysis The Architecture The Layering concepts , IoT Communication Pattern, IoT protocol Architecture, The 6LoWPAN Security aspects in IoT

UNIT-IV

IoT Application Development: Application Protocols MQTT, REST/HTTP, CoAP, MySQL Back-end Application Designing Apache for handling HTTP Requests, PHP & MySQL for data processing, MongoDB Object type Database, HTML, CSS &jQuery for UI Designing, JSON lib for data processing, Security & Privacy during development, Application Development for mobile Platforms: Overview of Android / IOS App Development tools

UNIT-V

Case Study & advanced IoT Applications: IoT applications in home, infrastructures, buildings, security, Industries, Home appliances, other IoT electronic equipments. Use of Big Data and Visualization in IoT, Industry 4.0 concepts. Sensors and sensor Node and interfacing using any Embedded target boards (Raspberry Pi / Intel Galileo/ARM Cortex/ Arduino)

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TEXT BOOKS

1. LoWPAN: The Wireless Embedded Internet, Zach Shelby, Carsten Bormann, Wiley
2. Internet of Things: Converging Technologies for Smart Environments and Integrated Ecosystems, Dr. OvidiuVermesan, Dr. Peter Friess, River Publishers
3. Interconnecting Smart Objects with IP: The Next Internet, Jean-Philippe Vasseur, Adam Dunkels, Morgan Kuffmann

REFERENCES

1. The Internet of Things: From RFID to the Next-Generation Pervasive Networked Lu Yan, Yan Zhang, Laurence T. Yang, HuanshengNing
2. Internet of Things (A Hands-on-Approach) , Vijay Madisetti , ArshdeepBahga
3. Designing the Internet of Things , Adrian McEwen (Author), Hakim Cassimally

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M.Tech. (I Sem.) **17VE06 - HIGH SPEED VLSI DESIGN**

L	T	P	Cr.
3	-	-	3

Pre-Requisites: VLSI Design

COURSE EDUCATIONAL OBJECTIVES:

In this course student will learn about the frequency and time metrics, various power and clock distribution techniques for ICs, and various Latching strategies used in ICs.

COURSE OUTCOMES: At the end of this course student will be able to

CO1 Analyze need for High speed VLSI design using frequency, time metrics.
CO2 Use power distribution on-chip for high speed chips.
CO3 Design signaling convention and circuits for on-chip transmission lines.
CO4 Resolve timing convention and synchronization issues on-chip.
CO5 Develop clocked, non clocked logic and latching strategies for high speed design.

UNIT-I

Introduction to high speed digital design: Frequency, time and distance issues in digital VLSI design. Capacitance and inductance effects, high speed properties of logic gates, speed and power. Modeling of wires, geometry and electrical properties of wires, Electrical models of wires, transmission lines, lossless LC transmission lines, lossy RLC transmission lines and special transmission lines.

UNIT-II

Power distribution and Noise: Power supply network, local power regulation, IR drops, area bonding. On-chip bypass capacitors and symbiotic bypass capacitors. Power supply isolation. Noise sources in digital systems, power supply noise, crosstalk and inter symbol interference.

UNIT-III

Signaling convention and circuits: Signaling modes for transmission lines, signaling over lumped transmission media, signaling over RC interconnect, driving lossy LC lines, simultaneous bi-directional signaling terminations, transmitter and receiver circuits.

UNIT-IV

Timing convention and synchronization: Timing fundamentals, timing properties of clocked storage elements, signals and events, open loop timing, level sensitive clocking, pipeline timing, closed loop timing, clock distribution, synchronization failure and meta-stability, clock distribution, clock skew and methods to reduce clock skew, controlling crosstalk in clock lines, delay adjustments, clock oscillators and clock jitter - PLL and DLL based clock aligners.

UNIT-V

Clocked & non clocked Logics:

Single-Rail Domino Logic, Dual-Rail Domino Structures, Latched Domino Structures, Clocked Pass GateLogic, Static CMOS, DCVS Logic, Non-Clocked Pass Gate Families.

Latching Strategies:

Basic Latch Design, and Latching single-ended logic and Differential Logic, Race Free Latches for Pre-charged Logic Asynchronous Latch Techniques

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TEXT BOOKS

1. William S. Dally & John W. Poulton, **"Digital Systems Engineering"**, *Cambridge University Press*, 1998.
2. Kerry Bernstein &et. Al., "**High Speed CMOS Design Styles"**, Kluwer, 1999.

REFERENCES

1. Howard Johnson & Martin Graham, **"High Speed Digital Design"** A Handbook of Black Magic, *Prentice Hall PTR*, 1993.
2. Masakazu Shoji, **"High Speed Digital Circuits"**, *Addison Wesley Publishing Company*, 1996.
3. Jan M, Rabaey, et al, **"Digital Integrated Circuits",** A Design Perspective, *Pearson*, 2003.

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M.Tech. (I Sem.) **17VE07 - IMAGE AND VIDEO PROCESSING**

L	T	P	Cr.
3	-	-	3

Pre-Requisites: Digital Image Processing

COURSE EDUCATIONAL OBJECTIVES:

In this course student will learn about the various compression, enhancement and segmentation techniques, image transformation techniques, and algorithms for 2D video signals.

COURSE OUTCOMES: At the end of this course student will be able to

CO1 Examine different image transformation techniques.
CO2 Evaluate various image enhancement and segmentation techniques.
CO3 Analyze different compression techniques for images.
CO4 Infer time-varying image formation models in video.
CO5 Compare 2-D motion estimation algorithms for video signals.

UNIT-I

Fundamentals of Image Processing and Image Transforms: Basic steps of Image Processing System Sampling and Quantization of an image – Basic relationship between pixels Image Transforms: 2 D- Discrete Fourier Transform, Discrete Cosine Transform (DCT), Wavelet Transforms: Continuous Wavelet Transform, Discrete Wavelet Transforms.

UNIT-II

Image Processing Techniques:

Image Enhancement: Spatial domain methods: Histogram processing, Fundamentals of Spatial filtering, Smoothing spatial filters, Sharpening spatial filters. Frequency domain methods: Basics of filtering in frequency domain, image smoothing, image sharpening, Selective filtering.

Image Segmentation: Segmentation concepts, Point, Line and Edge Detection, Thresholding, Region Based segmentation.

UNIT-III

Image Compression: Image compression fundamentals - Coding Redundancy, Spatial and Temporal redundancy, Compression models: Lossy & Lossless, Huffman coding, Arithmetic coding, LZW coding, Run length coding, Bit plane coding, Transform coding, Predictive coding, Wavelet coding, JPEG Standards.

UNIT-IV

Basic steps of Video Processing: Analog Video, Digital Video. Time-Varying Image Formation models: Three-Dimensional Motion Models, Geometric Image Formation, Photometric Image Formation, Sampling of Video signals, Filtering operations.

UNIT-V 2-D

Motion Estimation: Optical flow, General Methodologies, Pixel Based Motion Estimation, Block- Matching Algorithm, and Mesh based Motion Estimation, Global Motion Estimation, Region based Motion Estimation, Multi resolution motion estimation, Waveform based coding, Block based transform coding, Predictive coding, Application of motion estimation in Video coding.

TEXT BOOKS

1. Digital Image Processing – Gonzaleze and Woods, 3rd ed., Pearson.
2. Video processing and communication – Yao Wang, JoemOstermann and Ya–quin Zhang. 1st Ed., PH Int.

REFERENCE:

Digital Video Processing – M. Tekalp, Prentice Hall International

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M.Tech. (I Sem.) 17VE08 - SYSTEM MODELING AND SIMULATION

L	T	P	Cr.
3	-	-	3

Pre-Requisites: Random variables

COURSE EDUCATIONAL OBJECTIVES:

In this course student will learn about the various Simulation and Programming Models, Optimization methodologies.

COURSE OUTCOMES: At the end of this course student will be able to

CO1 Understand basic simulation models, characterizing and simulation diagrams.
CO2 Model time driven systems and stochastic processes.
CO3 Know how to simulate any discrete systems using queuing systems.
CO4 Discuss system optimization, modeling and simulation methodology.
CO5 Build simulation models with programming languages.

UNIT – I

Basic Simulation Modeling, Systems, Models and Simulation, Nature of Systems, event Driven Models, Simulation of Single Server Queuing System, event Driven Models, Characterizing Systems, Simulation Diagrams.

UNIT – II

Stochastic generators: Uniformly Distributed Random Numbers, Statistical Properties of U[0,1] generators, Generation of Non-Uniform and Arbitrary Random Variates, Random processes, Characterizing and Generating Random
Processes, White Noise. Modeling Time Driven Systems: Modeling Input Signals, Discrete and Distributed Delays, System Integration, Linear Systems.
Exogenous Signals and Events: Disturbance Signals, State Machines, Petri Nets and their Analysis, System Encapsulation.

UNIT – III

Markov Process: Probabilistic Models, Discrete Time Markov Processes, Random Walks, Poisson Processes, Exponential Distribution, Simulating a Poisson Process, Continuous Time Markov Process Event Driven Models: Simulation Diagrams, Queuing Theory, M/M/I Queues, Simulating Queuing Systems, Finite Capacity Queues, Multiple Servers, M/M/C Queues.

UNIT – IV

System Optimization: System Identification, Searches, Alpha / Beta trackers, Multidimensional Optimization, Modeling and Simulation Methodology.

UNIT – V

Simulation Software and Building Simulation Models:

Comparison of Simulation Packages with Programming Languages, Classification of Simulation Software, Desirable software features, General Purpose Simulation Packages-Arena, Extend; Guide lines for determining the level of Model detail, Techniques for increasing Model Viability and credibility.

TEXT BOOKS

1. System Modeling and Simulation: An Introduction – Frank L. Severance, 2001,John Wiley&Sons.
2. Simulation Modeling and Analysis - Averill M.Law, W.DavidKelton,3ed.,2003,TMH.

REFERENCES

Systems Simulation – Geoffery Gordan, PHI

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M.Tech. (I Sem.) **17VE09 - VLSI DESIGN AUTOMATION**

L	T	P	Cr.
3	-	-	3

Pre-Requisites: VLSI Design

COURSE EDUCATIONAL OBJECTIVES:

In this course student will learn about the design cycles, various techniques on Partitioning, Placement and Routing and addressing their problems.

COURSE OUTCOMES: At the end of this course student will be able to

CO1 Understand need for VLSI physical design automation.
CO2 Analyze VLSI automation algorithms for partitioning.
CO3 Formulate placement , floor planning and pin assignment problems and simulate.
CO4 Resolve routing issues using various algorithms.
CO5 Illustrate physical design cycle for FPGAs.

UNIT-I

VLSI Physical Design Automation: Introduction, VLSI Design cycle, new trends in VLSI design cycle, new trends in Physical design cycle, Design styles, full custom Basic terminology, complex issues, basic algorithms, Basic data structures, and algorithms.

UNIT-II

VLSI Automation Algorithms: Partitioning: problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms.

UNIT-III

Placement, Floor Planning & Pin Assignment: problem formulation, simulation base placement algorithms, other placement algorithms, constraint based floor planning, floor planning algorithms for mixed block & cell design. General & channel pin assignment

UNIT-IV

Global Routing: Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches

Detailed Routing: Problem formulation, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms.

Over The Cell Routing & Via Minimization: two layers over the cell routers, constrained & unconstrained via minimization

UNIT-V

Physical design Automation of FPGAs:

Introduction, FPGA Technologies, Physical design cycle for FPGAs, Partitioning, Routing, Routing algorithms for the non-segmented model, Routing algorithms for segmented model, routing algorithms for staggered model.

TEXT BOOK

NaveedShervani, **"Algorithms for VLSI physical design Automation"**, Springer Publisher, Third edition.

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REFERENCES

1. ChristophnMeinel& Thorsten Theobold, **"Algorithm and Data Structures for VLSI Design"**, KAP, 2002.
2. Rolf Drechsheler :**"Evolutionary Algorithm for VLSI"**, Second edition
3. Trimburger, **"Introduction to CAD for VLSI",** Kluwer Academic publisher, 2002

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M.Tech. (I Sem.) **17VE60 - DIGITAL VLSI SYSTEM DESIGN LAB**

L	T	P	Cr.
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Pre-Requisites: ECAD Lab

COURSE EDUCATIONAL OBJECTIVES:

In this course student will learn about the VHDL Programming of various Digital Circuits, design and implementation of various CMOS IC circuits using Mentor Graphics Tools.

COURSE OUTCOMES: At the end of this course student will be able to

CO1 Design CMOS Logic gates using Pyxis Schematic Editor.
CO2 Model digital modules using VHDL/Verilog and Simulate.
CO3 Verify Implementation of Digital Design on FPGA Board.

- Minimum of 10 programs from Part –I and 2 programs from Part -II are to be conducted.
- Design and implementation of the following CMOS digital circuits using Mentor Graphics /Xilinx CAD tools. The design shall include Gate-level design, Transistor-level design, Hierarchical design, Verilog HDL/VHDL design, Logic synthesis, Simulation and verification.

Part –I: VLSI Front End Design programs:

Programming can be done using any complier. Down load the programs on FPGA/CPLD boards and performance testing may be done using pattern generator (32 channels) and logic analyzer apart from verification by simulation with any of the front end tools.

1. Design of 8 input priority encoder and 3 to 8 Decoder
2. Design of 8x1Mux and 1x8 Demux
3. Design of 4 bit adder
4. Design 4 bit Magnitude Comparator
5. Design of BCD adder
6. Design of ALU
7. Design of D,T,JK Flip Flops
8. Design of Shift Registers
9. Design of Counters
10. Design of FSM(Moore's, Mealy Machines)
11. Design of Booth multiplier
12. Design of Electronic Dice game

Part –II: VLSI Back End Design programs:

- Design and implementation of the following CMOS digital/analog circuits using Cadence / Mentor Graphics / Synopsys / Equivalent CAD tools.
- The design shall include Gate-level design/Transistor level design/Hierarchical design/Verilog HDL or VHDL design, Logic synthesis, Simulation and verification, Scaling of CMOS Inverter for different technologies, study of secondary effects (temperature, power supply and process corners), Circuit optimization with respect to area, performance and/or power, Layout, Extraction of parasitics and back annotation, modifications in circuit parameters and layout consumption, DC/transient analysis, Verification of layouts (DRC, LVS).

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1. Introduction to layout design rules
2. Layout, physical verification, placement & route for complex design, static timing analysis, IR drop analysis and crosstalk analysis of the following:
- Basic logic gates
- CMOS inverter
- CMOS NOR/ NAND gates
- CMOS XOR and MUX gates
- CMOS 1-bit full adder
- Static / Dynamic logic circuit (register cell)
- Latch
- Pass transistor

3. Layout of any combinational circuit (complex CMOS logic gate)- Learning about data paths

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M.Tech. (I Sem.) **17VE61 - EMBEDDED SYSTEM DESIGN LAB**

Pre-Requisites: MPMC Lab

COURSE EDUCATIONAL OBJECTIVES:

In this course student will learn about the programming in Assembly language programs on ARM processor kits, programming on CPLD and FPGA kits using EDK Tools.

COURSE OUTCOMES: At the end of this course student will be able to

CO1 Develop the Assembly Language Programs for ARM processors.
CO2 Develop the interfacing programs for ARM processors and I/O devices.
CO3 Design an Embedded System using the FPGA and EDK tools.

- The following programs are to be implemented on **ARM based Processors/Equivalent.**
- **Minimum of 10 programs are to be conducted.**

1. ARM Assembly Language Programming-I
2. ARM Assembly Language Programming-II
3. Program to Interface 8 Bit LED
4. Program to demonstrate Time delay program using built in Timer/Counter feature
5. Program to Displaying a message in a 2 line x 16 Characters LCD display and verify the result in debug terminal.
6. Generation of PWM Signal
7. Serial Communication
8. Traffic light Controller
9. Stepper motor Controller
10. Basic Audio Processing on IDE environment.
11. Program to demonstrate I2C Interface on IDE environment
12. Program to implement Buzzer Interface on IDE environment

Part II

The following programs are to be implemented on **Xilinx FPGA Zynq 7000 series/Equivalent**.

- **Minimum of 2 programs are to be conducted.**

13. Design of System On Chip platform using Xilinx FPGAs and Embedded Development Kit Tools
14. Design dual processor based System on chip using Xilinx EDK Tools and Zynq 7000 series FPGA
15. Hardware Software co-design using Xilinx EDK Tools and Advanced FPGA Board Zynq 7000 series

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M.Tech. (I Sem.)	17VE90 - ADVANCED COMPUTER ARCHITECTURE	L	T	P	Cr.
		3	-	-	3

Pre-Requisites: Computer Organization & Architecture

COURSE EDUCATIONAL OBJECTIVES:

In this course student will learn about the classification of parallel architectures, mechanisms, general pipelining, vector processing and its architecture, multiprocessors and its interconnected networks, VLSI architectures and Data flow computers and their architectures.

COURSE OUTCOMES:

At the end of the course the student will be able to

1. Identify the differences between serial processing and parallel processing architectures and their applications.
2. Describe the functionality of pipelining and vector processor structures, hazards in various pipelining structures.
3. Develop the computer systems using SIMD processors with various interconnection networks.
4. Design the multi-processor systems with different memory configurations.
5. Analyze the working of Instruction flow computers and Data flow computers for VLSI computations.

UNIT – I: INTRODUCTION TO PARALLEL PROCESSING

Trends Towards Parallel Processing, Parallel Processing Mechanisms, Architectural Classification, Parallel Computer Structures, Pipeline Computers, Array Computers, Multi Processor Systems, Data Flow and New Concepts, Parallel Processing Applications.

UNIT – II: PRINCIPLES OF PIPELINING AND VECTOR PROCESSING

Principles of Linear Pipelining, General Pipelines and Reservation Tables, Interleaved Memory Organizations, Design of Pipelined Instruction Units, Instruction Prefetch and Branch Handling, Data Buffering and Busing Structures, Internal Forwarding and Register Tagging, Hazard Detection and Resolution, Job Sequencing and Collision Prevention, Characteristics of Vector Processing, Pipelined Vector Processing Methods.

UNIT –III: STRUCTURES AND ALGORITHMS FOR ARRAY PROCESSORS

SIMD Array Processors, SIMD Computer Organizations, Inter PE Communications, SIMD Interconnection Networks, Parallel Algorithms for Array Processors, SIMD Matrix Multiplication, Parallel Sorting on Array Processors, Associative Memory Organizations, Associative Processors.

UNIT – IV: MULTIPROCESSOR ARCHITECTURES

Functional Structures, Interconnection Networks, Parallel Memory Organizations, Interleaved Memory Configurations, Multi Cache Problems and Solutions, Multiprocessor Operating Systems, Exploiting Concurrency for Multiprocessing, Language Features to Exploit Parallelism, Detection of Parallelism in Programs.

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UNIT – V: DATA FLOW COMPUTERS AND VLSI COMPUTATIONS

Data Driven Computing and Languages, Data Flow Computer Architectures, VLSI Computing Structures, The Systolic Array Architecture, Reconfigurable Processor Array, VLSI Matrix Arithmetic Processors, VLSI Arithmetic Modules, Partitioned Matrix Algorithms, Matrix Arithmetic Pipelines.

TEXT BOOK

Kai Hwang and Faye A. Briggs, "Computer Architecture and Parallel Processing", McGraw Hill International Edition, 2000

REFERENCES

1. Sima D, Fountain T and Peter Kacsuk, "Advanced Computer Architectures: A Design Space Approach", Pearson Education, 2005
2. John L. Hennessy and David a. Patterson, "Computer Architecture A Quantitative Approach", Elsevier, Fourth Edition, 2008
3. Kai Hwang, "Advanced Computer Architecture: Parallelism, Scalability, Programmability", TMH, 2000

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M.Tech. (II Sem.) **17VE10 - ANALOG VLSI DESIGN**

L	T	P	Cr.
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PRE-REQUISITES: EDC

COURSE EDUCATIONAL OBJECTIVES:
In this course student will learn about the operation of MOS devices, design of Oscillators, Phase Locked Loops, Reference Generators and Data Converters.

COURSE OUTCOMES: At the end of the course, student will be able to
CO1: Understand the basic physics and operation of MOS devices.
CO2: Develop efficient analytical tools for quantifying the behavior of basic circuits by inspection.
CO3: Design of Oscillators and Phase Locked Loops.
CO4: Develop reference generators.
CO5: Implement efficient data converters.

UNIT - I
Basic MOS Device Physics: General considerations, MOS I/V Characteristics, second order effects, MOS device models.
Single stage Amplifier: CS stage with resistance load, divide connected load, current source load, triode load, CS stage with source degeneration, source follower, common-gate stage, cascade stage, choice of device models.

UNIT - II
Frequency response of CS stage: source follower, Common gate stage, Cascade stage and Difference pair. Noise in CS stage, C- G stage, source follower, cascade stage, differential pair.
Differential Amplifiers & Current Mirrors: Basic difference pair, common mode response, Differential pair with MOS loads, Gilbert cell. Basic current mirrors, Cascade mirrors, active current mirrors.

UNIT - III
Operational Amplifiers: One Stage OP-Amp. Two Stage OP-Amp, Gain boosting, Common Mode Feedback, Slew rate, Power Supply Rejection, Noise in Op Amps.
Oscillators and Phase Locked Loops: Ring Oscillators, LC Oscillators, VCO, Mathematical Model of VCO. Simple PLL, Charge pump PLL, Non-ideal effects in PLL, Delay locked loops and applications.

UNIT - IV
Band gap References and Switched capacitor Circuits: General Considerations, Supply Independent biasing, PTAT Current Generation, Constant Gm Biasing, Sampling Switches, Switched Capacitor Amplifiers.

UNIT - V
Data Converter Architectures: DAC & ADC Specifications, Resistor String DAC, R-2R Ladder Network, Current Steering DAC, Charge Scaling DAC, Cyclic DAC, Pipeline DAC, Flash ADC, Pipeline ADC, Integrating ADC, Successive Approximation ADC.

TEXT BOOK
"**Design of Analog CMOS Integrated Circuits**", Behzad Razavi, TMH, 2007
REFERENCE
"**CMOS Circuit Design, Layout and Simulation**", R. Jacob Baker, 3rd Edition, IEEE Press

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M.Tech. (II Sem.) **17VE11 - REAL TIME OPERATING SYSTEMS**

L	T	P	Cr.
3	-	-	3

PRE-REQUISITES: Embedded System Design

COURSE EDUCATIONAL OBJECTIVES: In this course student will learn about fundamental concepts of real time operating systems, operating system objects, services and I/O concepts, various interrupts and timers.

COURSE OUTCOMES: At the end of the course, student will be able to

CO1 Understand the basic set of commands and utilities in Linux/UNIX systems.
CO2 Explain the fundamental concepts of real-time operating systems.
CO3 Analyze real-time operating systems objects, services and I/O concepts.
CO4 Evaluate various Interrupts and Timers.
CO5 Design real time embedded systems using the concepts of RTOS.

UNIT – I

Introduction: Introduction to UNIX/LINUX, Overview of Commands, File I/O (open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

UNIT - II

Real Time Operating Systems: Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, Tasks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency. Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use

UNIT - III

Objects, Services and I/O Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem

UNIT - IV

Exceptions, Interrupts and Timers: Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT - V

RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, Tiny OS, and Basic Concepts of Android OS.

TEXT BOOK

Real Time Concepts for Embedded Systems – Qing Li, Elsevier, 2011

REFERENCES

1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2007, TMH.
2. Advanced UNIX Programming, Richard Stevens
3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh

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M.Tech. (II Sem.) **17VE12 - DSP PROCESSORS AND ARCHITECTURE**

L	T	P	Cr.
3	-	-	3

PRE-REQUISITES: SS and DSP

COURSE EDUCATIONAL OBJECTIVES: In this course student will learn about different computational parameters of DSP algorithms, architectural features of programmable DSP devices, interfacing capabilities and constructional requirements.

COURSE OUTCOMES: At the end of the course the student will be able to

CO 1: Analyze different computational parameters of DSP algorithms.
CO 2: Describe architectural features of programmable DSP devices.
CO 3: Compare specific constructional requirements of 54XX digital signal processors.
CO 4: Describe architectural features of analog devices family of DSP devices.
CO 5: Demonstrate interfacing capabilities of digital signal processors.

UNIT - I

Introduction To Digital Signal Processing: Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), linear time-invariant systems, Digital filters, Decimation and interpolation

Computational Accuracy in DSP Implementations: Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT - II

Architectures for Programmable DSP Devices: Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT - III

Programmable Digital Signal Processors: Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

UNIT - IV

Analog Devices Family of DSP Devices: Analog Devices Family of DSP Devices- ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP2100, ADSP-2181 high performance Processor.

Introduction to Blackfin Processor – The Blackfin Processor, Introduction to Micro Signal Architecture, Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals.

UNIT - V

Interfacing Memory And I/O Peripherals To Programmable DSP Devices: Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

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TEXT BOOKS

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. A Practical Approach to Digital Signal Processing – K Padmanabhan, R. Vijayarajeswaran, Ananthi.S, New Age International, 2006/2009.
3. Embedded Signal Processing with the Micro Signal Architecture Publisher: Woon-SengGan, Sen M. Kuo, Wiley-IEEE Press, 2007.

REFERENCES

1. Digital Signal Processors, Architecture, Programming and Applications – B. Venkataramani and M. Bhaskar, 2002, TMH.
2. Digital Signal Processing – Jonatham Stein, 2005, John Wiley.
3. DSP Processor Fundamentals, Architecture & Features- Lapsley et al. 2000, S. Chand & Co.
4. Digital Signal Processing Applications Using the ADSP-2100 Family by The Applications Enguneering Staff of Analog Devices, DSP Division, Edited by Amy Mar, PHI.
5. The Scientist and Engineering's Guide to Digital Signal Processing by Steven W. Smith, Ph.D., California Technical Publishing, ISBN 0-9660176-3-3, 1997.
6. Embedded Media Processing by David J. Katz and Rick Gentile of Analog Devices, Newnes, ISBN 0750679123, 2005.

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M.Tech. (II Sem.) **17VE13 - CMOS RF CIRCUIT DESIGN**

L	T	P	Cr.
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PRE-REQUISITES: CMOS Technology

COURSE EDUCATIONAL OBJECTIVES: In this course student will learn about CMOS RF circuit design, applications, complexity, various RF modulation and demodulation techniques, RF transmitter and receiver architectures, mixers, oscillators and frequency synthesizers.

COURSE OUTCOMES: At the end of the course, student will be able to
CO1: Describe CMOS RF Circuit design, applications and complexity
CO2: Compare various RF modulation and demodulation techniques
CO3: Analyze RF receiver and transmitter architectures
CO4: Design low noise amplifier, mixers and oscillators for RF transceivers
CO5: Choose power amplifiers and frequency synthesizers for RF transceivers

UNIT - I

Introduction to RF Design and Wireless Technology: Design and Applications, Complexity and Choice of Technology. Basic concepts in RF design: Nonlinearly and Time Variance, Inter symbol interference, random processes and noise. Sensitivity and dynamic range, passive impedance transformation.

UNIT - II

RF Modulation: Analog and digital modulation of RF circuits, Comparison of various techniques for power efficiency, Coherent and non-coherent detection, **Mobile RF communication** and basics of Multiple Access techniques.

UNIT - III

Receiver architectures: Heterodyne receivers, Homodyne receivers, Image-reject receivers, Digital-IF receivers, subsampling receivers, **Transmitter architectures**: Direct conversion and two-step transmitters, Receiver performance tests, case studies.

UNIT - IV

Low noise amplifiers and Mixers: Input matching, Bipolar LNAs, CMOS LNAs, Down conversion mixers: Biploar mixers, CMOS mixers, noise in mixers, **Oscillators**:Basic LC Oscillator topologies, voltage-controlled Oscillators, Phase noise, Bipolar and CMOS LC Oscillators, monolithic inductors, resonatorless VCOs, Quadrature signal generation, single sideband generation.

UNIT - V

Frequency Synthesizers: Phase locked loops, RF Synthesizer Architectures, Frequency dividers, **Power Amplifiers**: Linear and non-linear PAs, classification of power amplifiers, high frequency power amplifiers, large signal impedance matching, linearization techniques, Design examples

TEXT BOOKS

1. B. Razavi, "RF Microelectronics" PHI 1998
2. R. Jacob Baker, H.W. Li, D.E. Boyce "CMOS Circuit Design, layout and Simulation", PHI

REFERENCES

1. Thomas H. Lee "Design of CMOS RF Integrated Circuits" Cambridge University press 1998.
2. Y.P. Tsividis, "Mixed Analog and Digital Devices and Technology", TMH 1996

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M.Tech. (II Sem.) **17VE14 - EMBEDDED SOFTWARE DESIGN**

L	T	P	Cr.
3	-	-	3

PRE-REQUISITES: Embedded Systems and Operating Systems

COURSE EDUCATIONAL OBJECTIVES:
In this course student will learn about Operating systems concepts, programming concepts, programming in Linux and RT Linux.

COURSE OUTCOMES: At the end of the course, student will be able to
CO1 **Understand** the basic concepts of Operating Systems.
CO2 **Explain** the Programming concepts of RTOS.
CO3 **Analyze** various Case Studies for practical applications.
CO4 **Create** Target Image for Windows XP Embedded **& write** Programming in Linux.
CO5 **Write** Programming in RT Linux.

UNIT – I : Introduction
OS Services, Process Management, Timer Functions, Event Functions, Memory Management, Device, File and IO Systems Management, Interrupt Routines in RTOS Environment and Handling of Interrupt Source Calls, Real-Time Operating Systems, Basic Design Using an RTOS, RTOS Task Scheduling Models, Interrupt Latency and Response of the Tasks as Performance Metrics, OS Security Issues.

UNIT - II: RTOS Programming
Basic Functions and Types of RTOS for Embedded Systems, RTOS mCOS-II, RTOS Vx Works, Programming concepts of above RTOS with relevant Examples, Programming concepts of RTOS Windows CE, RTOS OSEK, RTOS Linux 2.6.x and RTOS RT Linux.

UNIT - III: Program Modeling – Case Studies
Case study of embedded system design and coding for an Automatic Chocolate Vending Machine (ACVM) Using Mucos RTOS, case study of digital camera hardware and software architecture, case study of coding for sending application layer byte streams on a TCP/IP Network Using RTOS Vx Works, Case Study of Embedded System for an Adaptive Cruise Control (ACC) System in Car, Case Study of Embedded System for a Smart Card, Case Study of Embedded System of Mobile Phone Software for Key Inputs.

UNIT - IV: Target Image Creation & Programming in Linux
Off-The-Shelf Operating Systems, Operating System Software, Target Image Creation for Window XP Embedded, Porting RTOS on a Micro Controller based Development Board. Overview and programming concepts of Unix/Linux Programming, Shell Programming, System Programming.

UNIT - V: Programming in RT Linux
Overview of RT Linux, Core RT Linux API, Program to display a message periodically, semaphore management, Mutex, Management, Case Study of Appliance Control by RT Linux System.

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TEXT BOOKS

1. Dr. K.V.K.K. Prasad: "Embedded/Real-Time Systems" Dream Tech Publications, Black pad book.
2. Rajkamal: "Embedded Systems-Architecture, Programming and Design", Tata McGraw Hill Publications, Second Edition, 2008.

REFERENCES

1. Labrosse, "Embedding system building blocks ", CMP publishers.
2. Rob Williams," Real time Systems Development", Butterworth Heinemann Publications.

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M.Tech. (II Sem.) **17VE15 - VLSI TESTING AND VERIFICATION**

L	T	P	Cr.
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PRE-REQUISITES: None

COURSE EDUCATIONAL OBJECTIVES: In this course student will learn about testable design, test generation algorithms for combinational and sequential circuits, design verification and verification tools, timing and physical design verification.

COURSE OUTCOMES: At the end of the course, student will be able to

CO1 Identify the significance of testable design
CO2 Implement combinational and sequential circuit test generation algorithms
CO3 Understand the importance of Design verification.
CO4 Learn verification tools.
CO5 Analyze the static timing verification and physical design verification.

UNIT - I

Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends Affecting Testing. Faults in Digital Circuits: Failures and Faults, Modeling of Faults, Temporary Faults.

Test Generation for Combinational Logic Circuits: Fault Diagnosis of Digital Circuits, Test Generation Techniques for Combinational Circuits, Detection of Multiple Faults in Combinational Logic Circuits.

UNIT - II

Design of Testable Sequential Circuits: Controllability and Observability, Ad Hoc Design Rules for Improving Testability, Design of Diagnosable Sequential Circuits, The Scan-Path Technique for Testable Sequential Circuit Design, Level-Sensitive Scan Design, Random Access Scan Technique, Partial Scan, Testable Sequential Circuit Design Using Nonscan Techniques, CrossCheck, Boundry Scan. Built-In Self Test: Test Pattern Generation for BIST, Output Response Analysis, Circular BIST, BIST Architectures.

UNIT - III

Testable Memory Design: RAM Fault Models, Test Algorithms for RAMs, Detection of Pattern Sensitive Faults, BIST Techniques for Ram Chips, Test Generation and BIST for Embedded RAMs.

Importance of Design Verification: What is verification? What is a test bench? The importance of verification, Reconvergence model, Formal verification, Equivalence checking, Model checking, Functional verification.[Ref2- Chapter1]

UNIT - IV

Verification Tools: Linting tools: Limitations of linting tools, lintingverilog source code, linting VHDL source code, lintingOpenVera and esource code, code reviews. Simulators: Stimulus and response, Event based simulation, cycle based simulation, Co-simulators, verification intellectual property: hardware modelers, waveform viewers.[Ref2-Chapter2]

The verification plan: The role of verification plan: specifying the verification plan, defining the first success. Levels of verification: unit level verification, reusable components verification, ASIC and FPGA verification, system level verification, board level verification, verifying strategies, verifying responses. [Ref2-Chapter3]

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UNIT - V

Static Timing Verification: Concept of static timing analysis. Cross talk and noise. Limitations of STA. slew of a wave form, Skew between the signals, Timing arcs and unateness, Min and Max timing paths, clock domains, operating conditions, critical path analysis, falsepaths, Timing models. [Ref3 Chapter 1, 2, 3, 8]

Physical Design Verification: Layout rule checks and electrical rule checks. Parasitic extraction. Antenna, Crosstalk and Noise**:** Cross talk glitch analysis, crosstalk delay analysis, timing verification [Ref4 Chapter 8]

TEXT BOOKS

1. P. K. Lala, **"Digital Circuit Testing and Testability"**, Academic Press
2. M.L. Bushnell and V.D. Agrawal, **"Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits"**, Kluwar Academic Publishers.

REFERENCES

1. M. Abramovici, M.A. Breuer and A.D. Friedman, **"Digital Systems and Testable Design"**, Jaico Publishing House, 2002.
2. JanickBergeron, **"Writing testbenches: functional verification of HDL models"**, 2nd edition ,Kluwer Academic Publishers,2003
3. JayaramBhasker,RakeshChadha ,**"Static Timing Analysis for Nanometer Designs"** A practical approach, Springer publications
4. PrakashRashinkar, PeterPaterson,Leena Singh **"System on a Chip Verification"**, Kulwer Publications.

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M.Tech. (II Sem.)	17VE16 - VLSI ARCHITECTURE FOR SIGNAL PROCESSING	L	T	P	Cr.
		3	-	-	3

PRE-REQUISITES: DSP

COURSE EDUCATIONAL OBJECTIVES: In this course student will learn about the fundamentals of VLSI signal processing and expose them to examples of applications. Design and optimize VLSI architectures for basic DSP algorithms.

COURSE OUTCOMES: At the end of the course, student will be able to
CO1: Understand VLSI design methodology for signal processing systems.
CO2: Differentiate between folding and unfolding architectures.
CO3: Elaborate various Systolic Array structures.
CO4: Analyze the VLSI algorithms and architectures for DSP.
CO5: Implement basic architectures for DSP using CAD tools.

UNIT - I
Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms
Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power , Retiming: Introduction – Definitions and Properties – Solving System of Inequalities – Retiming Techniques

UNIT – II
Folding and Unfolding: Folding: Introduction -Folding Transform - Register minimization Techniques – Register minimization in folded architectures – folding of multirate systems Unfolding: Introduction – An Algorithm for Unfolding – Properties of Unfolding – critical Path, Unfolding and Retiming – Applications of Unfolding

UNIT - III
Systolic Architecture Design: Introduction – Systolic Array Design Methodology – FIR Systolic Arrays – Selection of Scheduling Vector – Matrix Multiplication and 2D Systolic Array Design – Systolic Design for Space Representations contain Delays

UNIT - IV
Fast Convolution: Introduction – Cook-Toom Algorithm – Winograd algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

UNIT - V
Low Power Design: Scaling Vs Power Consumption –Power Analysis, Power Reduction techniques – Power Estimation Approaches Programmable DSP: Evaluation of Programmable Digital Signal Processors, DSP Processors for Mobile and Wireless Communications, Processors for Multimedia Signal Processing

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TEXT BOOKS

1. VLSI Digital Signal Processing- System Design and Implementation – Keshab K. Parhi, 1998, Wiley Inter Science.
2. VLSI and Modern Signal Processing – Kung S. Y, H. J. While House, T. Kailath, 1985, Prentice Hall.

REFERENCES

1. Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing – Jose E. France, YannisTsividis, 1994, Prentice Hall.
2. VLSI Digital Signal Processing – Medisetti V. K, 1995, IEEE Press (NY), USA.

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M.Tech. (II Sem.) **17VE17 - SOC DESIGN**

L	T	P	Cr.
3	-	-	3

PRE-REQUISITES: VLSI Technology

COURSE EDUCATIONAL OBJECTIVES: In this course student will learn about the SOC design, embedded memories, interconnect architectures of SOC.

COURSE OUTCOMES: At the end of the course, student will be able to

CO1: Understand the SOC designs
CO2: Comprehend the SOC design process
CO3: Evaluate embedded memories
CO4: Analyze interconnect architectures of SOC
CO5: Remembering the MPSoCs

UNIT - I

Motivation for SoC Design - Review of Moore"s law and CMOS scaling, benefits of system-on-chip integration in terms of cost, power, and performance. Comparison on System-on-Board, System-on-Chip, and System-in-Package. Typical goals in SoC design – cost reduction, power reduction, design effort reduction, performance maximization. Productivity gap issues and the ways to improve the gap – IP based design and design reuse.

UNIT - II

System On Chip Design Process: A canonical SoC Design, SoCDesignflow, waterfall vs spiral, top down vs bottom up, Specification requirement, Types of Specification, System Design Process, System level design issues, Soft IP vs Hard IP, IP verification and Integration, Hardware-Software codesign, Design for timing closure, Logic design issues, Verification strategy, On chip buses and interfaces, Low Power, Hardware Accelerators in Soc.

UNIT - III

Embedded Memories –cache memories, flash memories, embedded DRAM. Topics related to cache memories. Cache coherence.MESI protocol and Directory-based coherence.

UNIT - IV

Interconnect architectures for SoC. Bus architecture and its limitations. Network on Chip (NOC) topologies.Mesh-based NoC. Routing in anNoC. Packet switching and wormhole routing.

UNIT - V

MPSoCs: What, Why, How MPSoCs, Techniques for designing MPSoCs, Performance and flexibility for MPSoCs design

Case Study: A Low Power Open Multimedia Application Platform for 3G Wireless.

TEXT BOOKS

1. SudeepPasricha and NikilDutt,**"On-Chip Communication Architectures: System on Chip Interconnect"**, Morgan Kaufmann Publishers © 2008.
2. Rao R. Tummala, MadhavanSwaminathan, **"Introduction to system on package sop-Miniaturization of the Entire System"**, McGraw-Hill, 2008.

REFERENCES

1. James K. Peckol, **"Embedded Systems: A Contemporary Design Tool"**, Wiley Student Edition.
2. Michael Keating, Pierre Bricaud, **"Reuse Methodology Manual for System on Chip designs"**, Kluwer Accademic Publishers, 2nd edition, 2008.

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M.Tech. (II Sem.)	17VE18 - WIRELESS COMMUNICATIONS & NETWORKS	L	T	P	Cr.
		3	-	-	3

PRE-REQUISITES: Communication Systems

COURSE EDUCATIONAL OBJECTIVES:

In this course student will learn about wireless components, wireless networks, wireless system architecture, protocols, Mobile IP, Adhoc networks, digital audio and video broadcasting for high speed internet access.

COURSE OUTCOMES:

At the end of the course, student will be able to

CO1: Discuss about wireless components and wireless networks.
CO2: Describe System architecture and medium access control protocols.
CO3: Explain Mobile IP and mobile Adhoc networks.
CO4: Compare different transport layer protocols.
CO5: Analyze requirements of digital audio and video broadcasting for high-speed internet access.

UNIT - I

Introduction to Mobile and Wireless Landscape: Definition of Mobile and Wireless, Components of Wireless Environment, Challenges, Applications, Overview of Wireless Networks, Categories of Wireless Networks, open Research topics.
Wireless LAN: Infrared Vs Radio transmission, Infrastructure and Ad-hoc Network,
IEEE 802.11: System architecture, Protocol architecture. **Bluetooth:** User scenarios, Architecture.

UNIT - II

Global System for Mobile Communications (GSM): Introduction, Mobile services, System architecture, Radio interface, Localization and calling, Handover, Security.
(Wireless) Medium Access Control: Motivation for a specialized MAC (Hidden and exposed terminals, Near and far terminals), SDMA, FDMA, TDMA, CDMA.

UNIT - III

Mobile Network Layer:
Mobile IP: Goals, assumptions, entities and terminology, IP packet delivery, agent advertisement and discovery, registration, tunneling and encapsulation, optimizations, Dynamic Host Configuration Protocol (DHCP).
Mobile Ad hoc Networks (MANETs): Overview, Properties of a MANET, spectrum of MANET applications, routing and various routing algorithms.

UNIT - IV

Mobile Transport Layer: Traditional TCP, Indirect TCP, Snooping TCP, Mobile TCP, Fast retransmit/fast recovery, Transmission /time-out freezing, Selective retransmission, Transaction oriented TCP.

UNIT - V

Broadcast Systems: Overview, Cyclical repetition of data, Digital audio broadcasting: Multimedia object transfer protocol, Digital video broadcasting: DVB data broadcasting, DVB for high-speed internet access, Convergence of broadcasting and mobile communications.

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TEXT BOOK

Jochen Schiller, "Mobile Communications", Pearson Education, Second Edition, 2009.

REFERENCES

1. MartynMallick, "Mobile and Wireless Design Essentials", Wiley, 2008.
2. Asoke K Talukder, et al, "Mobile Computing", Tata McGraw Hill, 2008.
3. Mobile Computing, Raj Kamal,Oxford University Press.
4. William Stallings, " Wireless Communications & Networks", Person, Second Edition, 2007.
5. JimGeier, "Wireless Networks first-step", Pearson, 2005.

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M.Tech. (II Sem.) **17VE62 - ANALOG VLSI DESIGN LAB**

L	T	P	Cr.
-	-	2	1

PRE-REQUISITES: PSPICE knowledge

COURSE EDUCATIONAL OBJECTIVES: In this course student will learn about the design of basic building blocks of analog VLSI chips, cascade amplifiers and operational trans-conductance amplifier using CMOS technology.

COURSE OUTCOMES: At the end of the course, student will be able to
CO1: Design basic building blocks of analog VLSI Chips
CO2: Design cascade amplifier using CMOS Technology
CO3: Design operational Trans-conductance amplifier (OTA) using CMOS Technology

Minimum of 10 experiments are to be conducted using Cadence/Mentor Graphics/ Synopsys/ Equivalent CAD Tools

1. Trans conductance plots (voltage bias, current bias and technology bias).
2. Design of basic amplifier.
3. Design of cascode amplifier.
4. Design of basic current sink.
5. Design current sink by using negative feed back resistor
6. Design of cascode current sink.
7. Design of positive feed back boot strap current sink.
8. Design of regulated cascode current sink.
9. Design of simple current mirror
10. Design of cascode current mirror.
11. Design of wilson current mirror.
12. Design of widlar current mirror.
13. Design of 9 transistors operational transconductance amplifier.

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M.Tech. (II Sem.) **17VE63 - REAL TIME OPERATING SYSTEMS LAB**

L	T	P	Cr.
-	-	2	1

PRE-REQUISITES: Knowledge on Operating Systems

COURSE EDUCATIONAL OBJECTIVES: In this course student will learn about multitasking applications using RTOS, porting Linux on FPGA and create applications using ARM's Real Time Operating system.

COURSE OUTCOMES: At the end of the course, student will be able to
CO1: Develop multitasking applications using RTOS
CO2: Porting Linux on Zynq FPGA to develop embedded applications
CO3: Create applications using ARM's Real Time Operating System RTX

Minimum of 10 experiments are to be conducted using Xilinx EDK/ MicroVision IDE Keil

Write the following programs to understand the use of RTOS with ARM Processor on IDE Environment using ARM Tool chain and Library:

1. Create an application that creates two tasks that wait on a timer whilst the main task loops.
2. Write an application that creates a task which is scheduled when a button is pressed, which illustrates the use of an event set between an ISR and a task
3. Write an application that Demonstrates the interruptible ISRs(Requires timer to have higher priority than external interrupt button)

4(a) Write an application to Test message queues and memory blocks.
(b) Write an application to Test byte queues

5. Write an application that creates two tasks of the same priority and sets the time slice period to illustrate time slicing.

Interfacing Programs:

6. Write an application that creates a two task to Blinking two different LEDs at different timings
7. Write an application that creates a two task displaying two different messages in LCD display in two lines.
8. Sending messages to mailbox by one task and reading the message from mailbox by another task.
9. Sending message to PC through serial port by three different tasks on priority Basis.
10. Porting Linux and developing simple application on Xilinx Zed board
11. Developing image processing application with Linux OS on Xilinx Zynq FPGA
12. Simulating a stepper-motor driver
13. Write simple applications using RTX (ARM Keil's real time operating system, RTOS).

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M.Tech. (II Sem.)	17VE91 - ASIC DESIGN	L	T	P	Cr.
		3	-	-	3

PRE-REQUISITES: CPLD & FPGA

COURSE EDUCATIONAL OBJECTIVES : In this course student will learn about ASIC design flow, architecture of ASIC library design, programmable ASIC logic cells, logic synthesis and physical design phases.

COURSE OUTCOMES : At the end of the course, student will be able to

CO1: Acquire Knowledge on ASIC design flow
CO2: Analyze the architecture of ASIC library designs
CO3: Understanding the programmable ASIC logic cells
CO4: Analyzing the Logic synthesis in HDLs
CO5: Comprehend the physical design phases

UNIT - I

Types of ASICs – Design flow – Economics of ASICs – ASIC cell libraries – CMOS logic: CMOS Transistors, The CMOS process, CMOS design rules, Combinational logic cells, sequential logic cells, data path logic cells – I/O cells – cell compilers.

UNIT – II

ASIC Library design: Transistors as resistors – parasitic capacitance – logical effort, library cell design, library architecture, gate array design, standard cell design, data path cell design programmable ASICs: The Anti-fuse, Static RAM, EPROM and EEPROM Technology, practical issues, specifications.

UNIT - III

Programmable ASIC Design Software: Design systems – logic synthesis – half gate ASIC. Low level design entry: Schematic entry – low level design languages – PLA tools – EDIF – An overview of VHDL and Verilog.

UNIT – IV

Logic synthesis in Verilog and logic synthesis in VHDL, Finite –State machine synthesis, Memory synthesis, performance-Driven synthesis, Simulation: Types of simulation, The Comparator/MUX example, logic systems, how logic simulation works, cell models, delay models, Static Timing Analysis, formal verification, switch-level simulation, transistor level simulation.

UNIT – V

Floor planning & placement: Floor Planning Goals and Objectives, Measurement of Delay in floor planning, Floor planning tools, I/O and Power planning, Clock planning, Placement Algorithms. Routing: Global routing, Detailed routing, Special routing.

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TEXT BOOKS

1. Application specific Integrated Circuits", J.S. Smith, Addison Wesley.
2. Principles of CMOS VLSI Design : A System Perspective, N. Westle& K. Eshraghian, Addison – Wesley Pub.Co.1985.

REFERENCES

1. Basic VLSI Design :Systems and Circuits, Douglas A. Pucknell& Kamran Eshraghian, Prentice Hall of India Private Ltd. , New Delhi , 1989.
2. Introduction to VLSI System,C. Mead & L. Canway, Addison Wesley Pub
3. Introduction to NMOS & VLSI System Design, A. Mukharjee, Prentice Hall,
4. The Design & Analysis of VLSI Circuits, L. A. Glassey& D. W. Dobbepahl, Addison Wesley Pub Co. 1985.
5. Digital Integrated Circuits: A Design Perspective, Jan A. Rabey, Prentice Hall of India Pvt Ltd.

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M.Tech. (III Sem.) 17VE19 - DESIGN OF SEMICONDUCTOR MEMORIES

L	T	P	Cr.
3	-	-	3

PRE-REQUISITES: Computer Organization

COURSE EDUCATIONAL OBJECTIVES:

In this course student will learn about the structure and operation of the main types of semiconductor memory. The different contexts in which memories are tested together with the corresponding different types of tests.

COURSE OUTCOMES: At the end of the course, student will be able to

CO1 Understand memory cell structures and fabrication technologies.
CO2 Demonstrate application–specific memories and architectures.
CO3 Analyze memory design, fault modeling and test algorithms, limitations, and trade–offs
CO4 Illustrate general reliability issues of memory.
CO5 Elaborate various effects of radiation on memory

UNIT - I: Random Access Memory Technologies

SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM.

UNIT - II: Non-volatile Memories

Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture

UNIT - III: Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance

RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, nonvolatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory

UNIT - IV: Semiconductor Memory Reliability and Radiation Effects

General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test structures

UNIT - V: Advanced Memory Technologies and High-density Memory Packing Technologies

Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions.

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TEXT BOOK

Semiconductor Memories Technology – Ashok K. Sharma, 2002, Wiley.

REFERENCES

1. Advanced Semiconductor Memories – Architecture, Design and Applications - Ashok K. Sharma- 2002, Wiley.
2. Modern Semiconductor Devices for Integrated Circuits – Chenming C Hu, 1st Ed., Prentice Hall.

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M.Tech. (III Sem.) **17VE20 - EMBEDDED LINUX**

L	T	P	Cr.
3	-	-	3

PRE-REQUISITES: Operating Systems & Linux

COURSE EDUCATIONAL OBJECTIVES: In this course student will learn about embedded Linux, desktop Linux, embedded drivers for embedded applications, operating system porting, Linux real time programming.

COURSE OUTCOMES: At the end of the course, student will be able to
CO1: Compare Embedded Linux, desktop Linux and Embedded Linux distributions
CO2: Develop board support packages for optimized embedded storage space
CO3: Choose embedded drivers for typical embedded application
CO4: Analyze application porting and operating system porting
CO5: Describe Real-Time programming in linux /Hard Real-Time Linux

UNIT – I
Introduction: History of Embedded Linux, Embedded Linux versus Desktop Linux, Embedded Linux Distributions, Architecture of Embedded Linux, Linux Kernel Architecture, Linux Start-Up Sequence, GNU Cross-p\Platform Tool chain.

UNIT – II
Board Support Package: Inserting BSP in Kernel Build Procedure, Boot Loader Interface, Memory Map, Interrupt Management, PCI Subsystem, Timers, UART, and Power Management.
Embedded Storage: Flash Map, MTD—Memory Technology Device, MTD Architecture, Flash-Mapping Drivers, MTD Block and Character devices, Embedded File systems, Optimizing Storage Space.

UNIT – III
Embedded Drivers: Linux Serial Driver, Ethernet Driver, I2C subsystem on Linux, USB Gadgets, Watchdog Timer, and Kernel Modules.

UNIT - IV
Porting Applications: Architectural Comparison, Application Porting Road Map, Programming with Pthreads, Operating System Porting Layer (OSPL), Kernel API Driver.

UNIT - V
Real-Time Linux: Linux and Real-Time, Real-Time Programming in Linux, Hard Real-Time Linux.

TEXT BOOK
Embedded Linux System Design and Development, P.Raghavan, Amol Lad, Sriram Neelakandan, 2006, Auerbach Publications

REFERENCE BOOK
Embedded Linux – Hardware, Software and Interfacing

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M.Tech. (III Sem.) **17VE21 - MULTIMEDIA SYSTEMS**

L	T	P	Cr.
3	-	-	3

PRE-REQUISITES: None

COURSE EDUCATIONAL OBJECTIVES: In this course student will learn about in-depth understanding for multimedia communication standards and compression techniques. In-depth understanding for representation of image, video.

COURSE OUTCOMES: At the end of the course, student will be able to

CO1: Understand different multimedia communication devices.
CO2: Analyze different multimedia compression techniques.
CO3: Illustrate fundamental concepts of multimedia building blocks.
CO4: Demonstrate a diverse portfolio that reflects multimedia aesthetic proficiency.
CO5: Elaborate a set of professional skills and competencies in their practice of multimedia communication.

UNIT - I

Introduction to Multimedia: Multimedia, World Wide Web, Overview of Multimedia Tools, Multimedia Authoring, Graphics/ Image Data Types, and File Formats. Color in Image and Video: Color Science – Image Formation, Camera Systems, Gamma Correction, Color Matching Functions, CIE Chromaticity Diagram, Color Monitor Specifications, Outof- Gamut Colors, White Point Correction, XYZ to RGB Transform, Transform with Gamma Correction, L*A*B* Color Model. Color Models in Images – RGB Color Model for CRT Displays, Subtractive Color: CMY Color Model, Transformation from RGB to CMY, Under Color Removal: CMYK System, Printer Gamuts, Color Models in Video – Video Color Transforms, YUV Color Model, YIQ Color Model, Ycbcr Color Model.

UNIT - II

Video Concepts: Types of Video Signals, Analog Video, Digital Video. Audio Concepts: Digitization of Sound, Quantization and Transmission of Audio.

UNIT - III

Compression Algorithms: Lossless Compression Algorithms: Run Length Coding, Variable Length Coding, Arithmetic Coding, Lossless JPEG, Image Compression. Lossy Image Compression Algorithms: Transform Coding: KLT And DCT Coding, Wavelet Based Coding. Image Compression Standards: JPEG and JPEG2000.

UNIT - IV

Video Compression Techniques: Introduction to Video Compression, Video Compression Based on Motion Compensation, Search for Motion Vectors, H.261- Intra-Frame and InterFrameCoding, Quantization, Encoder and Decoder, Overview of MPEG1 and MPEG2.

UNIT - V

Audio Compression Techniques: ADPCM in Speech Coding, G.726 ADPCM, Vocoders – Phase Insensitivity, Channel Vocoder, Formant Vocoder, Linear Predictive Coding, CELP, Hybrid Excitation, Vocoders, MPEG Audio – MPEG Layers, MPEG Audio Strategy, MPEGAudio Compression Algorithms, MPEG-2 AAC, MPEG-4 Audio.

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TEXT BOOKS

1. Fundamentals of Multimedia – Ze- Nian Li, Mark S. Drew, PHI, 2010.
2. Multimedia Signals & Systems – Mrinal Kr. Mandal Springer International Edition 1st Edition, 2009

REFERENCES

1. Multimedia Communication Systems – Techniques, Stds&Netwroks K.R. Rao, Zorans. Bojkoric, DragoradA.Milovanovic, 1st Edition, 2002.
2. Fundamentals of Multimedia Ze- Nian Li, Mark S.Drew, Pearson Education (LPE), 1st Edition, 2009.
3. Multimedia Systems John F. KoegelBufond Pearson Education (LPE), 1st Edition, 2003.
4. Digital Video Processing – A. Murat Tekalp, PHI, 1996.
5. Video Processing and Communications – Yaowang, JornOstermann, Ya-QinZhang, Pearson, 2002.

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M.Tech. (III Sem.) **17VE22 - MEMS DESIGN AND FABRICATION**

L	T	P	Cr.
3	-	-	3

PRE-REQUISITES: None

COURSE EDUCATIONAL OBJECTIVES:

In this course student will learn about Micro-systems, Micro-fabrication. Mechanics for MEMS design, Electrostatic actuators and Electromagnetic actuators, various sensor structures.

COURSE OUTCOMES:

At the end of the course, student will be able to

CO1: Describe MEMS, Microsystems and Micro-fabrication
CO2: Analyze mechanics for MEMS Design
CO3: Distinguish Electrostatic actuators and Electromagnetic actuators
CO4: Model various circuits for MEMS Design
CO5: Choose Micro-bridge gas sensors, Piezo resistive Pressure Sensor and Bio-Chemical Sensors

UNIT – I

INTRODUCTION TO MEMS

MEMS and Microsystems:- Miniaturization and Typical products - Micro Sensors, Micro actuation - MEMS with micro actuators - Microaccelorometers and Micro fluidics - MEMS materials - Microfabrication.

UNIT – II

MECHANICS FOR MEMS DESIGN

Elasticity, stress, strain and material properties, Bending of thin plates, Spring configurations, torsional deflection, Mechanical vibration, Resonance - Thermo mechanics – Actuators, force and response time, Fracture and thin film mechanics, material, Physical Vapor Deposition (PVD), Chemical Mechanical Polishing (CMP).

UNIT – III

ELECTROSTATIC DESIGN

Electrostatics:- basic theory, electro static instability, Surface tension, gap and finger pull up - Electro static actuators - Comb generators - Gap closers - Rotary motors - Inch worms - Electromagnetic actuators - Bistable actuators.

UNIT – IV

CIRCUIT MODELING OF MEMS

Circuit modeling of MEMS:- Resonator equivalent circuit, Thermal Circuits and Fluidic Circuits – Signal Conditioning Circuits:- Op-Amp models and Circuits, transistor level-design – Electronic and Mechanical Noise:- Electronic noise sources, Brownian motion noise, circuit noise calculation procedure, SNR and dynamic range.

UNIT – V

CASE STUDIES

Microbridge gas sensors – Piezoelectric rate gyroscope – Capacitive Accelerometer – Piezoresistive Pressure Sensor – Thermal Sensors:- Radiation Sensors, Mechanical Sensors and Bio-Chemical Sensors.

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TEXT BOOK

Santeria, S., "Microsystems Design", Kluwer publishers, 2000.

REFERENCES

1. Maluf, N., "An Introduction to Micro Electro Mechanical System Design", Artech House, 2000.
2. Gad-el-Hak, M., "The MEMS Handbook", CRC press Baco Raton, 2000.
3. Hsu, T.R., "MEMS and Micro systems Design and Manufacture" Tata McGraw-Hill, New Delhi, 2002.
4. Gardner, J.W., Vijay k. varadan, V.K. and Osama O.Awadelkarim, "Micro Sensors MEMS and Smart Devices", John Wiley and son LTD, 2002
5 Allen, J.J., "Micro Electro Mechanical System Design", CRC Press published in 2005.

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M.Tech. (III Sem.) **17VE23 - NANO ELECTRONICS**

L	T	P	Cr.
3	-	-	3

PRE-REQUISITES: None

COURSE EDUCATIONAL OBJECTIVES: In this course student will learn about nano science and engineering, fabrication methods, techniques for characterization of nano structures, properties of nano particles, carbon nano structures, applications of nano electronics.

COURSE OUTCOMES: At the end of the course, student will be able to
CO1: Distinguish Nano science and engineering and fabrication methods
CO2: Discuss techniques for characterization of nanostructures
CO3: Illustrate fabrication techniques and physical processes
CO4: Describe properties of nanoparticles, carbon Nano structures
CO5: Classify Nano Electronics applications in NEMS, QWIP and optical memories

UNIT - I

Introduction: Overview of nanoscience and engineering. Development milestones in microfabrication and electronic industry. Moore's law and continued miniaturization., Classification of Nanostructures, Electronic properties of atoms and solids: Isolated atom, Bonding between atoms, Giant molecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices, Electronic conduction, effects of nanometer length scale, Fabrication methods: Top down processes, Bottom up processes methods for templating the growth of nanomaterial's, ordering of Nano systems.

UNIT - II

Characterization: Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, diffraction techniques: bulk, surface, spectroscopy techniques: photon, radiofrequency, electron, surface analysis and depth profiling: electron, mass, Ion beam, Reflectrometry, Techniques for property measurement: mechanical, electron, magnetic, thermal properties.

Inorganic semiconductor nanostructures: overview of semiconductor physics. Quantum confinement in semiconductor nanostructures: quantum wells, quantum wires, quantum dots, super-lattices, band offsets, electronic density of states.

UNIT - III

Fabrication techniques: requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching, cleaved edge over growth, growth of vicinal substrates, strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum wells, semiconductor nanocrystals, collidal quantum dots, self-assembly techniques.

Physical processes: modulation doping, quantum hall effect, resonant tunneling, charging effects, ballistic carrier transport, Inter band absorption, intra band absorption, Light emission processes, phonon bottleneck, quantum confined stark effect, nonlinear effects, coherence and De phasing, characterization of semiconductor nanostructures: optical electrical and structural.

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UNIT - IV

Methods of measuring properties structure:atomic, crystallography, microscopy, spectroscopy. Properties of nanoparticles: metal nanoclusters, semiconducting nanoparticles, rare gas and molecular clusters, methods of synthesis(RF, chemical, thermolysis, pulsed laser methods) Carbon nanostructures and its applications(field emission and shielding, computers, fuel cells, sensors, catalysis).Self assembling nanostructured molecular materials and devices: building blocks, principles of self-assembly, methods to prepare and pattern nanoparticles, templated nanostructures, Liquid crystal mesophases. Nanomagnetic materials and devices: magnetism, materials, magneto resistance, nanomagnetism in technology, challenges facing nanomagnetism.

UNIT - V

Applications: Inject ion lasers, quantum cascade lasers, single photon sources, biological tagging, optical memories, coulomb blockade devices, photonic structures, QWIP's, NEMS, MEMS.

TEXT BOOK

Ed Robert Kelsall, IanHamley, MarkGeoghegan, **" Nanoscale science and technology"** ,John wiley and sons,2007.

REFERENCES

1. Charles P Poole,Jr,Frank J owens, **"Introduction to Nanotechnology"** ,John wiley,copyright 2006,Reprint 2011.
2. Ed William A Goddard III,Donald W Brenner,SergeyEdwardLyshevski,Gerald J Lafrate, **" Hand Book of Nanoscience Engineering and Technology"** ,CRC press,2003

LBRCE EXAM CELL Dt.....

HEAD
Department of Electronics & Communication Engineering
Lakireddy Bali Reddy College of Engineering
MYLAVARAM. Krishna Dt., Andhra Pradesh

M.Tech. (III Sem.) **17VE24 - LOW POWER VLSI DESIGN**

L	T	P	Cr.
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PRE-REQUISITES: VLSI Design

COURSE EDUCATIONAL OBJECTIVES: In this course student will learn about concepts of power consumption, power analysis, low power design, and low power architectural level methodologies.

COURSE OUTCOMES: At the end of the course, student will be able to
CO1: Understand the concepts of power consumptions
CO2: Analyze the power analysis
CO3: Create low power design circuits
CO4: Comprehend the low power systems
CO5: Evaluate the Architectural Level Methodologies

UNIT - I
Introduction: Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches, Physics of power dissipation in CMOS devices.
Device & Technology Impact on Low Power: Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.

UNIT - II
Power estimation, Simulation Power analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation.
Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

UNIT - III
Low Power Design Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library.
Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic.

UNIT - IV
Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.
Low power Clock Distribution: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network.

UNIT - V
Algorithm & Architectural Level Methodologies: Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis.

TEXT BOOK
Rabaey, Pedram, "**Low Power Design Methodologies**" Kluwer Academic, 1997

REFERENCES
1. Kaushik Roy, Sharat Prasad, "**Low-Power CMOS VLSI Circuit Design**" Wiley, 2000
2. Gary K. Yeap, "**Practical Low Power Digital VLSI Design**", KAP, 2002.

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