COURSE STRUCTURE

I SEMESTER

Subject code	Name of the Subject	Contact hours/week		Credits	Scheme of Valuation		Total Marks
		L	P		Internal (CIE)	External (SEE)	
MTVL101	VLSI Technology and Design	4		3	40	60	100
MTVL102	CPLD and FPGA Architectures and Applications	4		3	40	60	100
MTVL103	Microcontrollers for Embedded System Design	4		3	40	60	100
MTVL104	Embedded Real Time Operating Systems	4		3	40	60	100
	Program Elective-I						
MTVL1051	Wireless Communications & Networks	4		3	40	60	100
MTVL1052	VLSI Design Automation						
MTVL1053	Nano Electronics						
	Program Elective-II						
MTVL1061	Modern DSP	4		3	40	60	100
MTVL1062	Embedded Linux and Basics of Device Drivers						
MTVL1063	High Speed VLSI Design						
MTVL151	VLSI Design Lab		3	2	25	50	75
MTVL152	Technical Seminar		3	2	75		75
	Total	**24**	**6**	**22**	**340**	**410**	**750**

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II SEMESTER

Subject code	Name of the Subject	Contact hours/week		Credits	Scheme of Valuation		Total Marks
		L	P		Internal (CIE)	External (SEE)	
MTVL201	Low Power VLSI Design	4		3	40	60	100
MTVL202	Design of Analog and Mixed Mode VLSI Circuits	4		3	40	60	100
MTVL203	Cryptography and Network Security	4		3	40	60	100
MTVL204	Advanced Embedded Systems	4		3	40	60	100
MTVL2051 MTVL2052 MTVL2053	**Program Elective-III** System Modeling and Simulation VLSI Architectures for Signal Processing Digital Signal Processors and Architectures	4		3	40	60	100
MTVL2061 MTVL2062 MTVL2063	**Program Elective-IV** Internet of Things System-on-Chip Design VLSI Testing and Verification	4		3	40	60	100
MTVL251	Embedded Systems Lab		3	2	25	50	75
MTVL252	Mini Project		3	2	75		75
	Total	**24**	**6**	**22**	**340**	**410**	**750**

III & IV SEMESTERS

Subject code	Name of the Subject	Contact hours/week		Credits	Scheme of Valuation		Total Marks
		L	P		Internal (CIE)	External (SEE)	
MTVL351	Dissertation			40	50	150	200
	Total			40	50	150	200

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I SEMESTER

MTVL101-VLSI TECHNOLOGY AND DESIGN

Lecture	**: 4 Periods/week**	**Internal Marks**	**: 40**
		External Marks	**: 60**
Credits	**: 3**	**External Examination**	**: 3 Hrs**

UNIT-I:

Review of Microelectronics and Introduction to MOS Technologies: MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS &BiCMOS Circuits: Ids-Vds relationships, Threshold Voltage Vt, Gm, Gds and ωo, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT-II

Layout Design and Tools: Transistor structures, Wires and Bias, Scalable Design rules, Layout Design and Tools.

Logic Gates & Layouts: Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT-III

Combinational Circuit Design: Delay Estimation, Logical Effort and Transistor Sizing, Power Dissipation, Circuit Families, Circuit Pitfalls, Low-power Logic Design, Comparison of Circuit Families, Silicon-on-Insulator Circuit Design

UNIT-IV

Sequential Circuit Design: Introduction, Sequencing Static Circuits, Circuit Design of Latches and Flip-flops: Conventional CMOS Latches and Flip-Flops, Pulsed Latches, Resettable Latches and Flip-Flops, Enabled Latches and Flip-flops. Static Sequencing Element Methodology: Choice of Elements, Low-power Sequential Design. Synchronizers: A simple synchronizer, arbiter.

UNIT-V

Floor Planning and System Design : Floor planning methods, Global interconnect, Floor Plan design, off-chip connections, Register Transfer Design, Pipelining

TEXT BOOKS

1. Essentials of VLSI Circuits and Systems, K. Eshraghian. D, A.Pucknell, 2005, PHI.
2. Modern VLSI Design - Wayne Wolf, fourth edition, Pearson Education.
3. CMOS VLSI Design A Circuits and systems perspective Third Edition Neil H.E.Weste

REFERENCES

1. Introduction to VLSI systems – A Logic, Circuit and System Perspective- Ming Bo, Liu, CRC Press, 1st Edition 2011.
2. Principals of CMOS VLSI Design – N.H.E Weste, K.Eshraghian, 2nd ed., Adisson Wesley.

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MTVL103-MICRO CONTROLLERS FOR EMBEDDED SYSTEM DESIGN

Lecture	**: 4 Periods/week**	**Internal Marks**	**: 40**
		External Marks	**: 60**
Credits	**: 3**	**External Examination**	**: 3 Hrs**

UNIT – I

Introduction to Embedded Systems : Overview of Embedded Systems, Processor Embedded into a system, Embedded Hardware Units and Devices in system, Embedded Software, Complex System Design, Design Process in Embedded System, Formalization of System Design, Classification of Embedded Systems.

UNIT – II

Microcontrollers and Processor Architecture & Interfacing: 8051 Architecture. Real world interfacing, Introduction to advanced architectures, processor & memory organization, Instruction-level parallelism, and performance metrics.

UNIT – III

PIC Microcontroller Hardware : Introduction, Architectural overview, Memory organization, interrupts and reset, I/O ports, Timers

UNIT –IV

ARM Architecture : ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families.

Unit – V

Device Drivers & Interrupt service Mechanism : Programmed-I/O Busy-wait approach without ISM,ISR concept, Interrupt sources, Interrupt service mechanism, Multiple Interrupts, context and the periods for context switching, Interrupt latency and deadline, Classification of processors ISM from context-saving angle, Direct Memory Access, Device driver programming, Serial Bus communication protocols

TEXT BOOKS

1. Embedded Systems - Architecture Programming and Design – Raj Kamal, 2nd ed., 2008, TMH.
2. Embedded C Programming and the Microchip PIC-Richard Barnett, O" Cull, Cox, 2009, Cengage Learning.
3. ARM Systems Developer's Guides- Designing & Optimizing System Software – Andrew N. Sloss, Dominic Symes, Chris Wright, 2008, Elsevier.

REFERENCE BOOKS

1. Embedded Microcomputer Systems, Real Time Interfacing – Jonathan W. Valvano – Brookes Cole, 1999, Thomas Learning

MTVL102-CPLD AND FPGA ARCHITECTURE AND APPLICATIONS

Lecture	**: 4 Periods/week**	**Internal Marks**	**: 40**
		External Marks	**: 60**
Credits	**: 3**	**External Examination**	**: 3 Hrs**

UNIT - I

Introduction to Programmable Logic Devices: Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD Implementation of a Parallel Adder with Accumulation.

UNIT – II

Field Programmable Gate Arrays: Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, and Programmable I/O blocks in FPGAs, Dedicated specialized Components of FPGAs, and Applications of FPGAs.

UNIT – III

SRAM Programmable FPGAs: Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 And XC4000 Architectures.

UNIT – IV

Anti-Fuse Programmed FPGAs: Introduction, Programming Technology, Device Architecture, TheActel ACT1, ACT2 and ACT3 Architectures.

UNIT – V

Design Applications: General Design Issues, Counter Examples, A Fast Video Controller, A position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXTBOOKS

1. Field Programmable Gate Array Technology by Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design by Charles H. Roth Jr, LizyKurian John, Cengage Learning.

REFERENCE BOOKS

1. Field Programmable Gate Arrays by John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays by Pak K. Chan/SamihaMourad,
   Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs by Ian Grout, Elsevier, Newnes.
4. FPGA based System Design by Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

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MTVL104-EMBEDDED REAL TIME OPERATING SYSTEMS

Lecture	**: 4 Periods/week**	**Internal Marks**	**: 40**
		External Marks	**: 60**
Credits	**: 3**	**External Examination**	**: 3 Hrs**

UNIT – I

Introduction: Introduction to UNIX/LINUX, Overview of Commands, File I/O (open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

UNIT - II

Real Time Operating Systems: Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency. Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use

UNIT - III

Objects, Services and I/O

Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem

UNIT - IV

Exceptions, Interrupts and Timers: Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT V

RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, Tiny OS, and Basic Concepts of Android OS.

TEXT BOOK

1. Real Time Concepts for Embedded Systems – Qing Li, Elsevier, 2011

REFERENCE BOOKS

1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2007, TMH.
2. Advanced UNIX Programming, Richard Stevens
3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh

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MTVL1051-WIRELESS COMMUNICATIONS AND NETWORKS

Lecture	**: 4 Periods/week**	**Internal Marks**	**: 40**
		External Marks	**: 60**
Credits	**: 3**	**External Examination**	**: 3 Hrs**

UNIT-I

Wireless Communications & System Fundamentals: Introduction to wireless communications systems, examples, comparisons & trends, Cellular concepts-frequency reuse, strategies, interference & system capacity, trucking & grade of service, improving coverage &capacity in cellular systems.

UNIT-II

Multiple Access Techniques for Wireless Communication: FDMA, TDMA, SSMA (FHMA/CDMA/Hybrid techniques), SDMA technique (AS applicable to wireless communications).Packet radio access-protocols, CSMA protocols, reservation protocols, capture effect in packet radio, capacity of cellular systems.

UNIT-III

Wireless Networking: Introduction, differences in wireless & fixed telephone networks, traffic routing in wireless networks – circuit switching, packet switching X.25 protocol. **Wireless data services** – cellular digital packet data (CDPD), advanced radio data information systems, RAM mobile data (RMD). Common channel signaling (CCS), ISDN-Broad band ISDN & ATM, Signaling System no .7 (SS7)-protocols, network services part, user part, signaling traffic, services & performance

UNIT-IV

Mobile IP and Wireless Application Protocol: Mobile IP Operation of mobile IP, Co-located address, Registration, Tunneling, WAP Architecture, overview, WML scripts, WAP service, WAP session protocol, wireless transaction, Wireless datagram protocol.

Wireless LAN Technology Infrared LANs, Spread spectrum LANs, Narrow bank microwave LANs, IEEE 802 protocol Architecture, IEEE802 architecture and services, 802.11 medium access control, 802.11 physical layer.

UNIT-V

Mobile Data Networks: Introduction, Data oriented CDPD Network, GPRS and higher data rates, Short messaging service in GSM, Mobile application protocol.

Ad-hoc Wireless Networks: Cellular and Adhoc wireless networks, applications, MAC protocols, Routing, Multicasting, Transport layer Protocols, quality of service browsining, deployment considerations, Adhoc wireless Internet

TEXT BOOKS

1. Wireless Communication and Networking – William Stallings, 2003, PHI.
2. Wireless Communications, Principles, Practice-Theodore, S.Rappaport, 2nd Edn. 2002, PHI.
3. Principles of Wireless Networks – Kaveh Pah Laven and P. Krishna Murthy, 2002, PE

REFERENCES

1. Wireless Digital Communications – Kamilo Feher, 1999, PHI.
2. Telecommunication System Engineering – Roger L. Freeman, 4/ed., Wiley Interscience, John Wiley & Sons, 2004.

MTVL1052-VLSI DESIGN AUTOMATION

Lecture	**: 4 Periods/week**	**Internal Marks**	**: 40**
		External Marks	**: 60**
Credits	**: 4**	**External Examination**	**: 3 Hrs**

UNIT-I

Logic Synthesis & Verification: Introduction to combinational logic synthesis, Binary Decision Diagram, Hardware models for High-level synthesis.

UNIT-II

VLSI Automation Algorithms : Partitioning: problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms.

UNIT-III

Placement, Floor Planning & Pin Assignment : Problem formulation, simulation base placement algorithms, other placement algorithms, constraint based floor planning, floor planning algorithms for mixed block & cell design. General & channel pin assignment.

UNIT-IV

Global Routing: Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches
Detailed Routing: problem formulation, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms.
Over The Cell Routing & Via Minimization: two layers over the cell routers, constrained & unconstrained via minimization

UNIT-V

Scripting Languages: Overview of Scripting Languages – PERL, CGI, VB Script, Java Script. PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables. Inter process Communication Threads, Compilation & Line Interfacing

TEXT BOOKS

1. NaveedShervani, "Algorithms for VLSI physical design Automation", Kluwer Academic Publisher, Second edition.
2. ChristophnMeinel& Thorsten Theobold, "Algorithm and Data Structures for VLSI Design", KAP, 2002.

REFERENCE BOOKS

1. Rolf Drechsheler :"Evolutionary Algorithm for VLSI", Second edition
2. Trimburger, "Introduction to CAD for VLSI", Kluwer Academic publisher, 2002
3. Randal L, Schwartz Tom Phoenix, "Learning PERL", Oreilly Publications, 3rd Edn., 2000
4. Larry Wall, Tom Christiansen, John Orwant, "Programming PERL", Oreilly Publications, 3rd Edn., 2000.
5. Tom Christiansen, Nathan Torkington, "PERL Cookbook", Oreilly Publications, 3rd Edn,2000

MTVL1053-NANO ELECTRONICS

Lecture	**: 4 Periods/week**	**Internal Marks**	**: 40**
		External Marks	**: 60**
Credits	**: 3**	**External Examination**	**: 3 Hrs**

UNIT-I

Introduction: Overview of nanoscience and engineering. Development milestones in microfabrication and electronic industry. Moores law and continued miniaturization., Classification of Nanostructures, Electronic properties of atoms and solids: Isolated atom, Bonding between atoms, Giantmolecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices, Electronic conduction, effects of nanometerlength scale, Fabrication methods: Top down processes, Bottom up processes methods for templating the growth of nanomaterial's, ordering of Nano systems.

UNIT-II

Characterization: Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, spectroscopy techniques: photon, radiofrequency, electron, surface analysis and depth profiling: electron, mass, Ion beam, Reflectrometry, Techniques for property measurement: mechanical, electron, magnetic, thermal properties.

Inorganic semiconductor nanostructures: overview of semiconductor physics. Quantum confinement in semiconductor nanostructures: quantumwells, quantum wires, quantum dots, super-lattices, band offsets, electronicdensity of states.

UNIT-III

Fabrication techniques: requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching, cleaved edge over growth, growth of vicinal substrates, strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum wells, semiconductor nanocrystals, collidal quantum dots, self-assembly techniques.

UNIT-IV

Methods of measuring properties: Properties of nanoparticles: metalnanoclusters, semiconducting nanoparticles, rare gas and molecularclusters, methods of synthesis(RF, chemical, thermolysis, pulsed laser methods) Carbon nanostructures and its applications(field emission and shielding, computers, fuelcells, sensors, catalysis).Self assembling nanostructured molecular materials and devices: building blocks, principles of self-assembly, methods to prepare and pattern nanoparticles, template nanostructures, Liquid crystal mesophases. Nanomagnetic materials and devices: magnetism, materials, magnetoresistance, nanomagnetism in technology, challenges facing nanomagnetism.

UNIT-V

Applications: Injectionlasers, quantumcascadelasers, singlephotonsources, biologicaltagging, opticalmemories, coulomb blockade devices, photonic structures, QWIP's, NEMS, MEMS.

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TEXT BOOKS

1. Ed Robert Kelsall,IanHamley,MarkGeoghegan, " Nanoscale science and technology" ,John wiley and sons,2007.
2. Charles P Poole,Jr,Frank J owens, "Introduction to Nanotechnology" ,John wiley,copyright 2006,Reprint 2011.

REFERENCE BOOKS

1. Ed William A Goddard III,Donald W Brenner,SergeyEdwardLyshevski,Gerald J Lafrate, " Hand Book of Nanoscience Engineering and Technology" ,CRC press,2003

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MTVL1061-MODERN DSP

Lecture	**: 4 Periods/week**	**Internal Marks**	**: 40**
		External Marks	**: 60**
Credits	**: 3**	**External Examination**	**: 3 Hrs**

UNIT-I

Introduction and Discrete Fourier Transforms: Signals, Systems and Processing, Classification of Signals, The Concept of Frequency in Continuous-Time and Discrete-Time Signals, Analog-to-Digital and Digital-to-Analog Conversion, Frequency-Domain Sampling: The Discrete Fourier Transform, Properties of the DFT, Linear Filtering Methods Based on the DFT (Ref.1 Chap. 1 & 7)

UNIT-II

Design of Digital Filters: General Considerations, Design of FIR Filters, Design of IIR Filters from Analog Filters, Frequency Transformations.
(Ref.1Chap.10)

UNIT-III

Multirate Digital Signal Processing I: Introduction, EL Dimation by a factor 'D', Interpolation by a factor 'I', Sampling rate Conversion by a factor 'I/D', implementation of Sampling rate conversion, Multistage implementation of Sampling rate conversion

UNIT-IV

Multirate Digital Signal Processing II: Sampling rate conversion of Band Pass Signals, Sampling rate conversion by an arbitrary factor, Applications of Multirate Signal Processing, Digital Filter banks, Two Channel Quadrature Mirror Filter banks, M-Channel QMF bank. (Ref.1 Chap.11)

UNIT-V

Adaptive Filters: Applications of Adaptive Filters, Adaptive Direct Form FIR Filters- The LMS Algorithm, Adaptive Direct Form Filters-RLS Algorithm. (Ref.1 Chap.13)

TEXT BOOKS

1. Proakis and Manolakis, "Digital Signal Processing", Prentice Hall 1996. (Fourth Edition).
2. Roberto Cristi, "Modern Digital Signal Processing", Cengage Publishers, India, (Erstwhile Thompson Publications), 2003.

REFERENCE BOOKS

1. S.K. Mitra, "Digital Signal Processing: A Computer Based Approach", III Ed, Tata McGraw Hill, India, 2007.
2. E.C. Ifeachor and B W Jarvis, "Digital Signal Processing, a practitioners approach," II Edition, Pearson Education, India, 2002 Reprint

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MTVL1062-EMBEDDED LINUX AND BASICS OF DEVICE DRIVERS

Lecture	**: 4 Periods/week**	**Internal Marks**	**: 40**
		External Marks	**: 60**
Credits	**: 3**	**External Examination**	**: 3 Hrs**

UNIT–I

Introduction: History of Embedded Linux, Embedded Linux versus Desktop Linux, Embedded Linux Distributions, Architecture of Embedded Linux, Linux Kernel Architecture, Linux Start-Up Sequence, GNU Cross-p\Platform Tool chain.

UNIT–II

Board Support Package: Inserting BSP in Kernel Build Procedure, Boot Loader Interface, Memory Map, Interrupt Management, PCI Subsystem, Timers, UART, and Power Management.

Embedded Storage: Flash Map, MTD—Memory Technology Device, MTD Architecture, Flash-Mapping Drivers, MTD Block and Character devices, Embedded File systems, Optimizing Storage Space.

UNIT-III

Embedded Drivers: Linux Serial Driver, Ethernet Driver, I2C subsystem on Linux, USB Gadgets, Watchdog Timer, and Kernel Modules.

UNIT-IV

Porting Applications: Architectural Comparison, Application Porting Road Map, Programming with Pthreads, Operating System Porting Layer (OSPL), Kernel API Driver.

UNIT-V

Real-Time Linux: Linux and Real-Time, Real-Time Programming in Linux, Hard Real-Time Linux.

TEXT BOOK

1. Embedded Linux System Design and Development, P.Raghavan, Amol Lad, SriramNeelakandan, 2006, Auerbach Publications

REFERENCE BOOKS

1. Embedded Linux – Hardware, Software and Interfacing

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MTVL1063-HIGH SPEED VLSI DESIGN

Lecture	**: 4 Periods/week**	**Internal Marks**	**: 40**
		External Marks	**: 60**
Credits	**: 3**	**External Examination**	**: 3 Hrs**

UNIT-I

Introduction to high speed digital design: Frequency, time and distance issues in digital VLSI design. Capacitance and inductance effects, high speed properties of logic gates, speed and power. Modeling of wires, geometry and electrical properties of wires, Electrical models of wires, transmission lines, lossless LC transmission lines, lossy RLC transmission lines and special transmission lines.

UNIT-II

Power distribution and Noise: Power supply network, local power regulation, IR drops, area bonding. On-chip bypass capacitors and symbiotic bypass capacitors. Power supply isolation. Noise sources in digital systems, power supply noise, crosstalk and inter symbol interference.

UNIT-III

Signaling convention and circuits: Signaling modes for transmission lines, signaling over lumped transmission media, signaling over RC interconnect, driving lossy LC lines, simultaneous bi-directional signaling terminations, transmitter and receiver circuits.

UNIT-IV

Timing convention and synchronization: Timing fundamentals, timing properties of clocked storage elements, signals and events, open loop timing, level sensitive clocking, pipeline timing, closed loop timing, clock distribution, synchronization failure and meta-stability, clock distribution, clock skew and methods to reduce clock skew, controlling crosstalk in clock lines, delay adjustments, clock oscillators and clock jitter - PLL and DLL based clock aligners.

UNIT-V

Clocked & non clocked Logics: Single-Rail Domino Logic, Dual-Rail Domino Structures, Latched Domino Structures, Clocked Pass Gate Logic, Static CMOS, DCVS Logic, Non-Clocked Pass Gate Families.

Latching Strategies:

Basic Latch Design, and Latching single-ended logic and Differential Logic, Race Free Latches for Pre-charged Logic Asynchronous Latch Techniques

TEXT BOOKS

1. William S. Dally & John W. Poulton, "Digital Systems Engineering", Cambridge University Press, 1998.
2. Kerry Bernstein &et. Al., "High Speed CMOS Design Styles", Kluwer, 1999.

REFERENCE BOOKS

1. Howard Johnson & Martin Graham, "High Speed Digital Design" A Handbook of Black Magic, *Prentice Hall PTR*, 1993.
2. Masakazu Shoji, "High Speed Digital Circuits", Addison Wesley Publishing Company, 1996.
3. Jan M, Rabaey, et al, "Digital Integrated Circuits", A Design Perspective, Pearson, 2003.

MTVL151-VLSI DESIGN LABORATORY

Practical	**: 3 Periods/week**	**Internal Marks**	**: 25**
		External Marks	**: 50**
Credits	**: 2**	**External Examination**	**: 3 Hrs**

Note:

- Minimum of 10 programs from Part –I and 2 programs from Part -II are to be conducted.
- Design and implementation of the following CMOS digital/analog circuits using Cadence / Mentor Graphics / Synopsys / Equivalent CAD tools. The design shall include Gate-level design, Transistor-level design, Hierarchical design, Verilog HDL/VHDL design, Logic synthesis, Simulation and verification.

Part –I: VLSI Front End Design programs:

Programming can be done using any complier. Down load the programs on FPGA/CPLD boards and performance testing may be done using pattern generator (32 channels) and logic analyzer apart from verification by simulation with any of the front end tools.

1. HDL code to realize all the logic gates
2. Design and Simulation of adder, Serial Binary Adder, Multi Precession Adder, Carry Look Ahead Adder.
3. Design of 2-to-4 decoder
4. Design of 8-to-3 encoder (without and with parity)
5. Design of 8-to-1 multiplexer
6. Design of 4 bit binary to gray converter
7. Design of Multiplexer/ Demultiplexer, comparator
8. Design of Full adder using 3 modeling styles
9. Design of flip flops: SR, D, JK, T
10. Design of 4-bit binary, BCD counters (synchronous/ asynchronous reset) or any sequence counter
11. Design of a N- bit Register of Serial- in Serial –out, Serial in parallel out, Parallel in Serial out and Parallel in Parallel Out.
12. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
13. Design of 4- Bit Multiplier, Divider.
14. Design of ALU to Perform – ADD, SUB, AND-OR, 1's and 2's Compliment, Multiplication, and Division.
15. Design of Finite State Machine.
16. Implementing the above designs on Xilinx/Altera/Cypress/equivalent based FPGA/CPLD kits .

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Part –II: VLSI Back End Design programs:

- Design and implementation of the following CMOS digital/analog circuits using Cadence / Mentor Graphics / Synopsys / Equivalent CAD tools.
- The design shall include Gate-level design/Transistor level design/Hierarchical design/Verilog HDL or VHDL design, Logic synthesis, Simulation and verification, Scaling of CMOS Inverter for different technologies, study of secondary effects (temperature, power supply and process corners), Circuit optimization with respect to area, performance and/or power, Layout, Extraction of parasitics and back annotation, modifications in circuit parameters and layout consumption, DC/transient analysis, Verification of layouts (DRC, LVS).

1. Introduction to layout design rules

2. Layout, physical verification, placement & route for complex design, static timing analysis, IR drop analysis and crosstalk analysis of the following:

- Basic logic gates
- CMOS inverter
- CMOS NOR/ NAND gates
- CMOS XOR and MUX gates
- CMOS 1-bit full adder
- Static / Dynamic logic circuit (register cell)
- Latch
- Pass transistor

3. Layout of any combinational circuit (complex CMOS logic gate)- Learning ABOUT DATA PATHS

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II SEMESTER

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MTVL201-LOW POWER VLSI DESIGN

Lecture	**: 4 Periods/week**	**Internal Marks**	**: 40**
		External Marks	**: 60**
Credits	**: 3**	**External Examination**	**: 3 Hrs**

UNIT-I

Introduction: Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches, Physics of power dissipation in CMOS devices.

Device & Technology Impact on Low Power: Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.

UNIT-II

Power estimation, Simulation Power analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation.

Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

UNIT-III

Low Power Design Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library.

Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic.

UNIT- IV

Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.

Low power Clock Distribution: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network.

UNIT-V

Algorithm & Architectural Level Methodologies: Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis.

TEXT BOOK

1. Kaushik Roy, Sharat Prasad, "Low-Power CMOS VLSI Circuit Design" Wiley, 2000

REFERENCE BOOKS

1. Gary K. Yeap, "Practical Low Power Digital VLSI Design", KAP, 2002
2. Rabaey, Pedram, "Low Power Design Methodologies" Kluwer Academic, 1997

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MTVL202-DESIGN OF ANALOG AND MIXED MODE VLSI CIRCUITS

Lecture	**: 4 Periods/week**	**Internal Marks**	**: 40**
		External Marks	**: 60**
Credits	**: 3**	**External Examination**	**: 3 Hrs**

UNIT-I

Basic MOS Device Physics: General considerations, MOS I/V Characteristics, second order effects, MOS device models.

Single stage Amplifier: CS stage with resistance load, divide connected load, current source load, triode load, CS stage with source degeneration, source follower, common-gate stage, cascade stage, choice of device models.

UNIT-II

Frequency response of CS stage: source follower, Common gate stage, Cascade stage and Difference pair.Noise in CS stage, C- G stage, source follower, cascade stage, differential pair.

Differential Amplifiers & Current Mirrors: Basic difference pair, common mode response, Differential pair with MOS loads, Gilbert cell. Basic current mirrors, Cascade mirrors, active current mirrors.

UNIT-III

Operational Amplifiers: One Stage OP-Amp. Two Stage OP-Amp, Gain boosting, Common Mode Feedback, Slew rate, Power Supply Rejection, Noise in Op Amps.

Oscillators and Phase Locked Loops: Ring Oscillators, LC Oscillators, VCO, Mathematical Model of VCO. Simple PLL, Charge pump PLL, Non-ideal effects in PLL, Delay locked loops and applications.

UNIT-IV

BandgapReferncesand Switched capacitor Circuits: General Considerations, Supply Independent biasing, PTAT Current Generation, Constant Gm Biasing, Sampling Switches, Switched Capacitor Amplifiers.

UNIT-V

Data Converter Architecturres: DAC & ADC Specifications, Resistor String DAC, R-2R Ladder Network, Current Steering DAC, Charge Scaling DAC, Cyclic DAC, Pipeline DAC, Flash ADC, Pipeline ADC, Integrating ADC, Successive Approximation ADC.

TEXT BOOK

1. "Design of Analog CMOS Integrated Circuits", Behzad Razavi, TMH, 2007.

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MTVL203-CRYPTOGRAPHY & NETWORK SECURITY

Lecture	**: 4 Periods/week**	**Internal Marks**	**: 40**
		External Marks	**: 60**
Credits	**: 3**	**External Examination**	**: 3 Hrs**

UNIT-I

Introduction: Attacks, Services and Mechanisms, Security attacks, Security services, A Model for Internet work security. Classical Techniques: Conventional Encryption model, Steganography, Classical Encryption Techniques.

UNIT-II

Modern Techniques: Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations.

Algorithms: Triple DES, International Data Encryption algorithm, Blowfish, RC5, CAST-128, RC2, Characteristics of Advanced Symmetric block cifers.

Conventional Encryption: Placement of Encryption function, Traffic confidentiality, Key distribution, Random Number Generation.

Public Key Cryptography: Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange, Elliptic Curve Cryptography.

UNIT-III

Number theory: Prime and Relatively prime numbers, Modular arithmetic, Fermat's and Euler's theorems, Testing for primality, Euclid's Algorithm, the Chinese remainder theorem, Discrete logarithms.

Message authentication and Hash functions: Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash Functions and MACs

UNIT-IV

Hash and Mac Algorithms: MD File, Message digest Algorithm, Secure Hash Algorithm, RIPEMD-160, and HMAC. **Digital signatures and Authentication protocols**: Digital signatures, Authentication Protocols, Digital signature standards. **Authentication Applications**: Kerberos, X.509 directory Authentication service. Electronic Mail Security: Pretty Good Privacy, S/MIME.

UNIT-V

IP Security: Overview, Architecture, Authentication, Encapsulating Security Payload, Combining security Associations, Key Management

Web Security

Web Security requirements, Secure sockets layer and Transport layer security, Secure Electronic Transaction. **Intruders, Viruses and Worms:**Intruders, Viruses and Related threats. **Fire Walls** Fire wall Design Principles, Trusted systems.

TEXT BOOK

1. Cryptography and Network Security: Principles and Practice - William Stallings, 2000, PE.

REFERENCES

1. Principles of Network and Systems Administration, Mark Burgess,JohnWiel

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MTVL204-ADVANCED EMBEDDED SYSTEMS

Lecture	**: 4 Periods/week**	**Internal Marks**	**: 40**
		External Marks	**: 60**
Credits	**: 3**	**External Examination**	**: 3 Hrs**

UNIT-I

Typical Embedded System : Core of the Embedded System, Memory, Sensors and Actuators, Communication Interface, Embedded Firmware, Other System Components.

Characteristics and Quality Attributes of Embedded Systems: Hardware Software Co-Design and Program Modeling: Fundamental Issues in Hardware Software Co-Design, Computational Models in Embedded Design, Introduction to Unified Modeling Language, Hardware Software Trade-offs.

UNIT-II

Embedded Hardware Design and Development :EDA Tools, How to Use EDA Tool, Schematic Design – Place wire, Bus , port, junction, creating part numbers, Design Rules check, Bill of materials, Netlist creation , PCB Layout Design – Building blocks, Component placement, PCB track routing.

UNIT-III

ARM -32 bit Microcontroller family. Architecture of ARM Cortex M3 –General Purpose Registers, Stack Pointer, Link Register, Program Counter, Special Register,. Nested Vector Interrupt Controller. Interrupt behavior of ARM Cortex M3. Exceptions Programming.Advanced Programming Features.Memory Protection. Debug Architecture.

UNIT-IV

Embedded Firmware Design and Development: Embedded Firmware Design Approaches, Embedded Firmware Development Languages

Real-Time Operating System (RTOS) based Embedded System Design: Operating System Basics, Types of OS, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling, Threads, Processes and Scheduling: Putting them altogether, Task Communication, Task Synchronization, Device Drivers, How to Choose an RTOS

UNIT-V

The Embedded System Development Environment: The Integrated Development Environment (IDE), Types of Files Generated on Cross compilation, Disassembler /ELDompiler, Simulators, Emulators and Debugging, Target Hardware Debugging, Boundary Scan.

TEXT BOOK

1. Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education Private Limited, 2009

REFERENCE BOOKS

1. Joseph Yiu, "The Definitive Guide to the ARM Cortex-M3", Newnes, (Elsevier), 2008.
2. James K Peckol, "Embedded Systems – A contemporary Design Tool", John Weily, 2008.

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MTVL2051-SYSTEM MODELING AND SIMULATION

Lecture	**: 4 Periods/week**	**Internal Marks**	**: 40**
		External Marks	**: 60**
Credits	**: 3**	**External Examination**	**: 3 Hrs**

UNIT-I

Basic Simulation Modeling, Systems, Models and Simulation, Nature of Systems, event Driven Models, Simulation of Single Server Queuing System, event Driven Models, Characterizing Systems, Simulation Diagrams.

UNIT-II

Stochastic generators: Uniformly Distributed Random Numbers, Statistical Properties of U[0,1] generators, Generation of Non-Uniform and Arbitrary Random Variates, Random processes, Characterizing and Generating Random Processes, White Noise. Modeling Time Driven Systems: Modeling Input Signals, Discrete and Distributed Delays, System Integration, Linear Systems. Exogenous Signals and Events: Disturbance Signals, State Machines, Petri Nets and their Analysis, System Encapsulation.

UNIT-III

Markov Process: Probabilistic Models, Discrete Time Markov Processes, Random Walks, Poisson Processes, Exponential Distribution, Simulating a Poisson Process, Continuous Time Markov Process Event Driven Models: Simulation Diagrams, Queuing Theory, M/M/I Queues, Simulating Queuing Systems, Finite Capacity Queues, Multiple Servers, M/M/C Queues.

UNIT-IV

System Optimization: System Identification, Searches, Alpha / Beta trackers, Multidimensional Optimization, Modeling and Simulation Methodology.

UNIT-V

Simulation Software and Building Simulation Models:

Comparison of Simulation Packages with Programming Languages, Classification of Simulation Software, Desirable software features, General Purpose Simulation Packages-Arena, Extend; Guide lines for determining the level of Model detail, Techniques for increasing Model Viability and credibility.

TEXT BOOKS

1. System Modeling and Simulation: An Introduction – Frank L. Severance, 2001, JohnWiley&Sons.
2. Simulation Modeling and Analysis - Averill M.Law, W.DavidKelton, , 3 ed., 2003, TMH.

REFERENCES

1. Systems Simulation-Geoffery Gordan, PHI.

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MTVL2052-VLSI ARCHITECTURES FOR SIGNAL PROCESSING

Lecture	**: 4 Periods/week**	**Internal Marks**	**: 40**
		External Marks	**: 60**
Credits	**: 3**	**External Examination**	**: 3 Hrs**

UNIT-I

Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms

Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power , Retiming: Introduction – Definitions and Properties – Solving System of Inequalities – Retiming Techniques

UNIT–II

Folding and Unfolding: Folding: Introduction -Folding Transform - Register minimization Techniques – Register minimization in folded architectures – folding of multirate systems Unfolding: Introduction – An Algorithm for Unfolding – Properties of Unfolding – critical Path, Unfolding and Retiming – Applications of Unfolding

UNIT-III

Systolic Architecture Design: Introduction – Systolic Array Design Methodology – FIR Systolic Arrays – Selection of Scheduling Vector – Matrix Multiplication and 2D Systolic Array Design – Systolic Design for Space Representations contain Delays

UNIT-IV

Fast Convolution: Introduction – Cook-Toom Algorithm – Winograd algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

UNIT-V

Low Power Design: Scaling Vs Power Consumption –Power Analysis, Power Reduction techniques – Power Estimation Approaches Programmable DSP: Evaluation of Programmable Digital Signal Processors, DSP Processors for Mobile and Wireless Communications, Processors for Multimedia Signal Processing

TEXT BOOKS

1. VLSI Digital Signal Processing- System Design and Implementation – Keshab K. Parhi 1998, Wiley Inter Science.
2. VLSI and Modern Signal Processing – Kung S. Y, H. J. While House, T. Kailath, 1985, Prentice Hall.

REFERENCES

1. Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing – Jose E. France, YannisTsividis, 1994, Prentice Hall.
2. VLSI Digital Signal Processing – Medisetti V. K, 1995, IEEE Press (NY), USA.

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MTVL2053-DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES

Lecture	**: 4 Periods/week**	**Internal Marks**	**: 40**
		External Marks	**: 60**
Credits	**: 3**	**External Examination**	**: 3 Hrs**

UNIT-I

Introduction To Digital Signal Processing: Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), linear time-invariant systems, Digital filters, Decimation and interpolation

Computational Accuracy in DSP Implementations: Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT-II

Architectures for Programmable DSP Devices: Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT-III

Programmable Digital Signal Processors: Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

UNIT-IV

Analog Devices Family of DSP Devices: Analog Devices Family of DSP Devices- ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP2100, ADSP-2181 high performance Processor.

Introduction to Blackfin Processor – The Blackfin Processor, Introduction to Micro Signal Architecture, Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals.

UNIT-V

Interfacing Memory And I/O Peripherals To Programmable DSP Devices: Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

TEXT BOOKS

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. A Practical Approach to Digital Signal Processing – K Padmanabhan, R. Vijayarajeswaran, Ananthi.S, New Age International, 2006/2009.
3. Embedded Signal Processing with the Micro Signal Architecture Publisher: Woon-SengGan, Sen M. Kuo, Wiley-IEEE Press, 2007.

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REFERENCES

1. Digital Signal Processors, Architecture, Programming and Applications – B. Venkataramani and M. Bhaskar, 2002, TMH.
2. Digital Signal Processing – Jonatham Stein, 2005, John Wiley.
3. DSP Processor Fundamentals, Architecture & Features- Lapsley et al. 2000, S. Chand & Co.
4. Digital Signal Processing Applications Using the ADSP-2100 Family by The Applications Enguneering Staff of Analog Devices, DSP Division, Edited by Amy Mar, PHI.
5. The Scientist and Engineering's Guide to Digital Signal Processing by Steven W. Smith, Ph.D., California Technical Publishing, ISBN 0-9660176-3-3, 1997.
6. Embedded Media Processing by David J. Katz and Rick Gentile of Analog Devices, Newnes, ISBN 0750679123, 2005.

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MTVL2061-INTERNET OF THINGS (IOT)

Lecture	**: 4 Periods/week**	**Internal Marks**	**: 40**
		External Marks	**: 60**
Credits	**: 3**	**External Examination**	**: 3 Hrs**

UNIT-I

The IoT Networking Core :Technologies involved in IoT Development: Internet/Web and Networking Basics OSI Model, Data transfer referred with OSI Model, IP Addressing, Point to Point Data transfer, Point to Multi Point Data transfer & Network Topologies, Sub-netting, Network Topologies referred with Web, Introduction to Web Servers, Introduction to Cloud Computing

UNIT-II

IoT Platform overview : Overview of IoT supported Hardware platforms such as: Raspberry pi, ARM Cortex Processors, Arduino and Intel Galileo boards. Network Fundamentals: Overview and working principle of Wired Networking equipment's – Router, Switches, Overview and working principle of Wireless Networking equipment's – Access Points, Hubs etc. Linux Network configuration Concepts: Networking configurations in Linux Accessing Hardware & Device Files interactions.

UNIT-III

IoT Architecture: History of IoT, M2M – Machine to Machine, Web of Things, IoT protocols Applications: Remote Monitoring & Sensing, Remote Controlling, Performance Analysis The Architecture The Layering concepts , IoT Communication Pattern, IoT protocol Architecture, The6LoWPAN Security aspects in IoT

UNIT-IV

IoT Application Development: Application Protocols MQTT, REST/HTTP, CoAP, MySQL Back-end Application Designing Apache for handling HTTP Requests, PHP & MySQL for data processing, MongoDB Object type Database, HTML, CSS &jQuery for UI Designing, JSON lib for data processing, Security & Privacy during development, Application Development for mobile Platforms: Overview of Android / IOS App Development tools

UNIT-V

Case Study & advanced IoT Applications: IoT applications in home, infrastructures, buildings, security, Industries, Home appliances, other IoT electronic equipments. Use of Big Data and Visualization in IoT, Industry 4.0 concepts. Sensors and sensor Node and interfacing using any Embedded target boards (Raspberry Pi / Intel Galileo/ARM Cortex/ Arduino)

TEXT BOOKS

1. 6LoWPAN: The Wireless Embedded Internet, Zach Shelby, Carsten Bormann, Wiley
2. Internet of Things: Converging Technologies for Smart Environments and Integrated Ecosystems, Dr. OvidiuVermesan, Dr. Peter Friess, River Publishers

REFERENCES

1. The Internet of Things: From RFID to the Next-Generation Pervasive Networked Lu Yan, Yan Zhang, Laurence T. Yang, HuanshengNing
2. Internet of Things (A Hands-on-Approach) , Vijay Madisetti , ArshdeepBahga

MTVL2062-SYSTEM-ON-CHIP DESIGN

Lecture	**: 4 Periods/week**	**Internal Marks**	**: 40**
		External Marks	**: 60**
Credits	**: 3**	**External Examination**	**: 3 Hrs**

UNIT-I

Motivation for SoC Design - Review of Moore's law and CMOS scaling, benefits of system-on-chip integration in terms of cost, power, and performance. Comparison on System-on-Board, System-on-Chip, and System-in-Package. Typical goals in SoC design – cost reduction, power
reduction, design effort reduction, performance maximization. Productivity gap issues and the ways to improve the gap – IP based design and design reuse.

UNIT-II

System On Chip Design Process: A canonical SoC Design, SoC Design flow, waterfall vs spiral, top down vs bottom up, Specification requirement, Types of Specification, System Design Process, System level design issues, Soft IP vs Hard IP, IP verification and Integration, Hardware-Software codesign, Design for timing closure, Logic design issues, Verification strategy, On chip buses and interfaces, Low Power, Hardware Accelerators in Soc.

UNIT-III

Embedded Memories –cache memories, flash memories, embedded DRAM. Topics related to cache memories. Cache coherence. MESI protocol and Directory-based coherence.

UNIT-IV

Interconnect architectures for SoC. Bus architecture and its limitations. Network on Chip (NOC) topologies.Mesh-based NoC. Routing in anNoC. Packet switching and wormhole routing.

UNIT-V

MPSoCs: What, Why, How MPSoCs, Techniques for designing MPSoCs, Performance and flexibility for MPSoCs design

Case Study: A Low Power Open Multimedia Application Platform for 3G Wireless.

TEXT BOOKS

1. Sudeep Pasricha and NikilDutt,"On-Chip Communication Architectures: System on Chip Interconnect", Morgan Kaufmann Publishers © 2008.
2. Rao R. Tummala, MadhavanSwaminathan, "Introduction to system on package sop-Miniaturization of the Entire Syste", McGraw-Hill, 2008.

REFERENCES

1. James K. Peckol, "Embedded Systems: A Contemporary Design Tool", Wiley Student Edition.
2. Michael Keating, Pierre Bricaud, "**R**euse Methodology Manual for System on Chip designs", Kluwer Accademic Publishers, 2nd edition, 2008.
3. Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits", Tata Mcgraw-Hill, 3rd Edition.

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MTVL2063-VLSI TESTING AND VERIFICATION

Lecture	**: 4 Periods/week**	**Internal Marks**	**: 40**
		External Marks	**: 60**
Credits	**: 3**	**External Examination**	**: 3 Hrs**

UNIT-I

Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends Affecting Testing. Faults in Digital Circuits: Failures and Faults, Modeling of Faults, Temporary Faults.

Test Generation for Combinational Logic Circuits: Fault Diagnosis of Digital Circuits, Test Generation Techniques for Combinational Circuits, Detection of Multiple Fauls in Combinational Logic Circuits.

UNIT-II

Design of Testable Sequential Circuits: Controllability and Observability, Ad Hoc Design Rules for Improving Testability, Design of Dignosable Sequential Circuits, The Scan-Path Technique for Testable Sequential Circuit Design, Level-Sensitive Scan Design, Random Access Scan Technique, Partial Scan, Testable Sequential Circuit Design Using Nonscan Techniques, Cross Check, Boundry Scan. Built-In Self Test: Test Pattern Generation for BIST, Output Response Analysis, Circular BIST, BIST Architectures.

UNIT-III

Testable Memory Design: RAM Fault Models, Test Algorithms for RAMs, Detection of Pattern Sensitive Faults, BIST Techniques for Ram Chips, Test Generation and BIST for Embedded RAMs.

Importance of Design Verification: What is verification? What is attest bench? The importance of verification, Reconvergence model, Formal verification, Equivalence checking, Model checking, Functional verification.[Ref4- Chapter1]

UNIT-IV

Verification Tools: Linting tools: Limitations of linting tools, lintingverilog source code, linting VHDL source code, lintingOpenVera and esourcecode, code reviews. Simulators: Stimulus and response, Event based simulation, cycle based simulation, Co-simulators, verification intellectual property: hardware modelers, waveform viewers.[Ref4-Chapter2]

The verification plan: The role of verification plan: specifying the verification plan, defining the first success. Levels of verification: unit level verification, reusable components verification, ASIC and FPGA verification, system level verification, board level verification, verifying strategies, verifying responses. [Ref4-Chapter3]

UNIT-V

Static Timing Verification: Concept of static timing analysis. Cross talk and noise. Limitations of STA. slew of a wave form, Skew between the signals, Timing arcs and unateness, Min and Max timing paths, clock domains, operating conditions, critical path analysis, falsepaths, Timing models. [Ref5 Chapter 1, 2, 3, 8]

Physical Design Verification: Layout rule checks and electrical rule checks. Parasitic extraction. Antenna, Crosstalk and Noise: Cross talk glitch analysis, crosstalk delay analysis, timing verification [Ref6 Chapter 8]

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TEXT BOOKS

1. P. K. Lala, "Digital Circuit Testing and Testability", Academic Press
2. M.L. Bushnell and V.D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwar Academic Publishers.

REFERENCES

1. Abramovici, M.A. Breuer and A.D. Friedman, "Digital Systems and Testable Design", Jaico Publishing House, 2002.
2. JanickBergeron, "Writing testbenches: functional verification of HDL models", 2nd edition ,Kluwer Academic Publishers,2003
3. JayaramBhasker,RakeshChadha ,"Static Timing Analysis for Nanometer Designs" A practical approach, Springer publications
4. PrakashRashinkar, PeterPaterson,Leena Singh "System on a Chip Verification", Kulwer Publications.

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MTVL251-EMBEDDED SYSTEMS LABORATORY

Practical	**: 3 Periods/week**	**Internal Marks**	**: 25**
		External Marks	**: 50**
Credits	**: 2**	**External Examination**	**: 3 Hrs**

Note:

The following programs are to be implemented on ARM based Processors/Equivalent. **Minimum of 5 programs from Part –I and 5 programs from Part –II are to be conducted.**

Part III programs are compulsory

Part-I

The following Programs are to be implemented on ARM Processor

1. Simple Assembly Program for
   a. Addition | Subtraction | Multiplication | Division
   b. Operating Modes, System Calls and Interrupts
   c. Loops, Branches
2. Write an Assembly programs to configure and control General Purpose Input/Output (GPIO) port pins.
3. Write an Assembly programs to read digital values from external peripherals and execute them with the Target board.
4. Program for reading and writing of a file
5. Program to demonstrate Time delay program using built in Timer / Counter feature on IDE environment
6. Program demonstrates setting up interrupt handlers. Press button to generate an interrupt and trace the program flow with debug terminal.
7. Program to Interface 8 Bit LED and Switch Interface
8. Program to implement Buzzer Interface on IDE environment
9. Program to Displaying a message in a 2 line x 16 Characters LCD display and verify the result in debug terminal.
10. Program to demonstrate I2C Interface on IDE environment
11. Demonstration of Serial communication. Transmission from Kit and reception from PC using Serial Port on IDE environment use debug terminal to trace the program.
12. Generation of PWM Signal

Part-II

Write the following programs to understand the use of RTOS with ARM Processor on IDE Environment using ARM Tool chain and Library:

1. Create an application that creates two tasks that wait on a timer whilst the main task loops.
2. Write an application that creates a task which is scheduled when a button is pressed, which illustrates the use of an event set between an ISR and a task
3. Write an application that Demonstrates the interruptible ISRs(Requires timer to have higher priority than external interrupt button)

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4. a).Write an application to Test message queues and memory blocks.
   b).Write an application to Test byte queues
5. Write an application that creates two tasks of the same priority and sets the time slice period to illustrate time slicing.

Interfacing Programs:

6. Write an application that creates a two task to Blinking two different LEDs at different timings
7. Write an application that creates a two task displaying two different messages in LCD display in two lines.
8. Sending messages to mailbox by one task and reading the message from mailbox by another task.
9. Sending message to PC through serial port by three different tasks on priority Basis.
10. Basic Audio Processing on IDE environment.

Part-III

The following programs are to be implemented on Xilinx FPGA Zynq 7000 series/Equivalent.

1. Design of System On Chip platform using Xilinx FPGAs and Embedded Development Kit Tools
2. Design dual processor based System on chip using Xilinx EDK Tools and Zynq 7000 series FPGA
3. Hardware Software co-design using Xilinx EDK Tools and Advanced FPGA Board Zynq 7000 series

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