LAKIREDDY BALIREDDY COLLEGE OF ENGINEERING (AUTONOMOUS)

(Approved by AICTE, Accredited by NBA, Affiliated to JNTUK, Kakinada and ISO 9001: 2008 Certified)

ACADEMIC REGULATIONS, COURSE STRUCTURE AND DETAILED SYLLABUS



2010 - 2011

M.TECH – SYSTEMS AND SIGNAL PROCESSING DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

L.B.Reddy Nagar, MYLAVARAM – 521 230 Krishna District, Andhra Pradesh State

M.TECH(ECE - SYSTEMS AND SIGNAL PROCESSING) - COURSE STRUCTURE

I-SEMESTER

		Schen	Scheme of Instruction	uc	Scheme	Scheme of Examination		
Code No.	Name of the Course	Peri	Periods per Week		Maxi	Maximum Marks	Total	credits
		Lecture	Tutorial	Lab.	Internal	External		
MEC101	Advanced Digital Signal Processing	4	1	ı	40	09	100	4
MEC102	Transform Techniques	4	1	1	40	09	100	4
MEC103	VLSI Technology and Design	4	1	1	40	09	100	4
MEC104	Microcontrollers For Embedded System Design	4	1	1	40	09	100	4
	ELECTIVE – I	Y2.				8		
MEC1051 MEC1052	DSP Processers & Architecture Image and Video Processing	4	ı	1	40	09	100	4
	ELECTIVE – II							
MEC1061 MEC1062	Radar Signal Processing Bio – Medical Signal Processing	4	1		40	09	100	4
MEC151	Seminar	,	ı	က	20	1	20	2
MEC152	Advanced Digital Signal Processing Lab	1	1	3	40	09	100	2
	TOTAL	24		9	330	420	750	28
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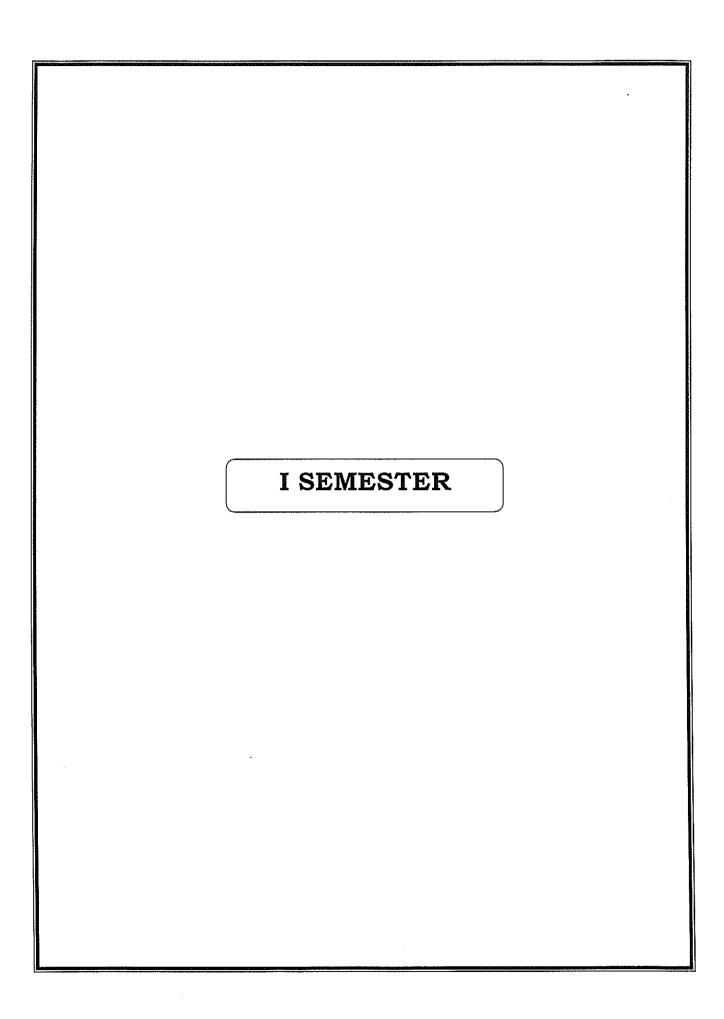
LAKIREDDY BALI REDDY COLLEGE OF ENGINEERING (AUTONOMOUS), MYLAVARAM - 521230

II-SEMESTER

MEC2051 MEC201 MEC203 MEC203 MEC203 MEC204 MEC204 MEC2051 MEC2061 Mireless Communication and NameC2062 MEC2061 MEC2061 MEC2061 MEC2061 Mireless Communication and NameC2062 MEC2061 MECZ061 ME		Schem	Scheme of Instruction	ction	Exami	Examination	-	1
		Perio	Periods per Week	ek	Maximu	Maximum Marks	lotal	credits
		Lecture	Tutorial	Lab	Internal	External		
	Processing	4	1	1	40	09	100	4
	ing	4	1	1	40	09	100	4
	w.	4	1	1	40	09	100	4
	nd Techniques	4	1	ŀ	40	09	100	4
Sec. 10 (100 to 100 to								
	CPLD & FPGA Architectures And Applications Design for Testability	4	1	I	40	09	100	4
0.00								
	Wireless Communication and Networks VLSI Signal Processing	4	'n	ı	40	09	100	4
		-	1	က	20	1	20	2
MEC208 Advanced ECAD Lab) Lab	1	1	3	40	09	100	2
TOT	TOTAL	24	1	9	330	420	750	28

III & IV SEMESTERS

		Schen	Scheme of Instruction	on	Scheme	Scheme of Examination		
Code No.	Name of the Course	Peri	Periods per Week		Max	Maximum Marks	Total	credits
		Lecture	Tutorial	Lab.	Internal	External		
WEC351	Technical Seminar	I	1	9	50		20	00
MEC451	Dissertation	1	1	15	20	150	200	24
* XXX	TOTAL	-	1	21	100	150	250	32
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M.TECH (SYSTI	M.TECH (SYSTEMS AND SIGNAL PROCESSING), A.Y.2010-2011		Page 15		- C	Lakireddy Bali Reddy College of Engineering ANDRAM Krishna Dt., Andhrapradesh.	eddy Colle Krishna D	ge or Engine t., Andhraprac



MEC101: ADVANCED DIGITAL SIGNAL PROCESSING

Lecture

: 4 Periods/week

Internal Marks

: 40

External Marks

: 60

Credits

: 4

External Examination

: 3 Hrs

UNIT - I

Review of DFT, FFT, IIR Filters, FIR Filters, Multirate Signal Processing: Introduction, Decimation by a factor D, Interpolation by a factor I, Sampling rate conversion by a rational factor I/D, Multistage Implementation of Sampling Rate Conversion, Filter design & Implementation for sampling rate conversion, Applications of Multirate Signal Processing

UNIT-II

Non-Parametric methods of Power Spectral Estimation: Estimation of spectra from finite duration observation of signals, Non-parametric Methods: Bartlett, Welch & Blackman & Tukey methods, Comparison of all Non-Parametric methods

UNIT - III

Parametric Methods of Power Spectrum Estimation: Autocorrelation & Its Properties, Relation between auto correlation & model parameters, AR Models - Yule-Waker & Burg Methods, MA & ARMA models for power spectrum estimation.

UNIT-IV

Linear Prediction: Forward and Backward Linear Prediction - Forward Linear Prediction. Backward Linear Prediction, Optimum reflection coefficients for the Lattice Forward and Backward Predictors. Solution of the Normal Equations: Levinson Durbin Algorithm, Schur Algorithm. Properties of Linear Prediction Filters

UNIT-V

Finite Word Length Effects: Analysis of finite word length effects in Fixed-point DSP systems - Fixed, Floating Point Arithmetic - ADC quantization noise & signal quality - Finite word length effect in IIR digital Filters - Finite word-length effects in FFT algorithms.

TEXTBOOKS

- Digital Signal Processing: Principles, Algorithms & Applications J.G.Proakis & 1. D.G.Manolokis, 4th ed., PHI.
- 2. Discrete Time signal processing -Alan V Oppenheim & Ronald W Schaffer, PHI.
- DSP A Pratical Approach Emmanuel C.Ifeacher, Barrie. W. Jervis, 2 ed., Pearson Education.

REFERENCES:

Modern spectral Estimation: Theory & Application – S. M. Kay, 1988, PH; Multirate Systems and Filter Banks – P.P. Vaidyanathan – Pearson Education

Digital Signal Processing - S.Salivahanan, A.Vallavaraj, C.Gnanapriya, 2000, HEAD

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MEC102: TRANSFORM TECHNIQUES

Lecture

: 4 Periods/week

Internal Marks

: 40

External Marks

: 60

Credits

: 4

External Examination

: 3 Hrs

UNIT - I

Review of Transforms: Signal spaces, concept of convergence, Hilbert spaces for energy signals, Fourier basis, FT-failure of FT-need for time-frequency analysis, spectrogram plot-phase space plot in time-frequency plane, Continuous FT, DTFT, Discrete Fourier Series and Transforms, Z-Transform, relation between CFT-DTFT, DTFT-DFS,DFS-DFT, DCT(1D&2D), Walsh, Hadamard, Haar, Slant, KLT,Hilbert Transforms — definition, properties and applications

UNIT - II

CWT & MRA: Time-frequency limitations, tiling of time-frequency plane for STFT, Heisenberg uncertainty principle, Short time Fourier Transform (STFT) analysis, short comings of STFT, Need for wavelets- Wavelet Basis- Concept of Scale and its relation with frequebcy, Continuous time wavelet Transform Equation- Series Expansion using Wavelets-CWT- Need for scaling Function- Multi resolution analysis, Tiling of time scale plane for CWT. Important Wavelets: Haar, Mexican Hat Meyer, Shannon, Daubechies.

UNIT - III

Multirate Systems, Filter Banks and DWT.

Basics of Decimation and Interpolation in time & frequency domains, Two-channel Filter bank, Perfect Reconstruction Condition, Relation ship between Filter Banks and Wavelet basis, DWT Filter Banks For Daubechies Wavelet Function

<u>UNIT – IV</u>

Special Topics: Wavelet Packet Transform Multidimensional Wavelets, Bi-orthogonal basis-B-splines, Lifting Scheme of Wavelet Generation, Multi Wavelets

UNIT - V

Applications of Transforms

Signal Denoising, Subband Coding of Speech and Music, Signal Compression - Use of DCT, DWT, KLT, 2-D DWT, Fractal Signal Analysis.

TEXT BOOKS

1. "Fundamentals of Wavelets- Theory, Algorithms and Applications", Jaideva C Goswami, Andrew K Chan, John Wiley & Sons, Inc, Singapore, 1999.

Wavelet Transforms-Introduction theory and applications-Raghuveer M.Rao and Ajit

S. Bopardikar, Pearson edu, Asia, New Delhi, 2003.

"Insight into Wavelets from Theory to practice ", Soman.K.P, Ramachandran. K.I, Printice Hall India, First Edition, 2004.

HEAD

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- 1. "Wavelets and sub-band coding", Vetterli M. Kovacevic, PJI, 1995.
- 2. "Introduction to Wavelets and Wavelet Transforms", C. Sydney Burrus, PHI, First Edition, 1997.
- 3. "A Wavelet Tour of Signal Processing", Stephen G. Mallat,. Academic Press, Second Edition,



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MEC103: VLSI TECHNOLOGY AND DESIGN

Lecture

: 4 Periods/week

Internal Marks

: 40

External Marks

: 60

Credits

External Examination : 3 Hrs

UNIT - I

Review of Microelectronics and Introduction to MOS Technologies: MOS, CMOS, BiCMOS Technology, Trends And Projections, Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: Ids-Vds relationships, Threshold Voltage Vt, Gm, Gds and ωo, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT - II

LAYOUT DESIGN AND TOOLS: Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

LOGIC GATES & LAYOUTS: Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT - III

COMBINATIONAL LOGIC NETWORKS: Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

UNIT-IV

SEQUENTIAL SYSTEMS: Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT - V

FLOOR PLANNING & ARCHITECTURE DESIGN: Floor planning methods, off-chip connections, High-level synthesis, Architecture for low power, SOCs and Embedded CPUs, Architecture testing.

TEXT BOOKS

- 1. Essentials of VLSI Circuits and Systems, K. Eshraghian Eshraghian. D, A.Pucknell,
- 2. Modern VLSI Design - Wayne Wolf, 3rd ed., 1997, Pearson Education.

REFERENCES

RCEPrincipals of CMOS VLSI Design - N.H.E Weste, K.Eshraghian, 2 ed., Adisson Wesley.

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M.TECH (SYSTEMS AND SIGNAL PROCESSING), A.Y.2010-2011

MEC104: MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN

Lecture

: 4 Periods/week

Internal Marks

: 40

External Marks

: 60

Credits

. 4

External Examination

: 3 Hrs

UNIT - I

Introduction to Embedded Systems Overview of Embedded Systems, Processor Embedded into a system, Embedded Hardware Units and Devices in system, Embedded Software, Complex System Design, Design Process in Embedded System, Formalization of System Design, Classification of Embedded Systems.

UNIT - II

Microcontrollers and Processor Architecture & Interfacing 8051 Architecture, Input/Output Ports and Circuits, External Memory, Counters and Timers, PIC Controllers. Interfacing Processor (8051, PIC), Memory Interfacing, I/O Devices, Memory Controller and Memory arbitration Schemes.

UNIT - III

Embedded RISC Processors & Embedded System-on Chip Processor PSOC (Programmable System-on-Chip) architectures, Continuous Timer blocks, Switched Capacitor blocks, I/O blocks, Digital blocks, Programming of PSOC, Embedded RISC Processor architecture – ARM Processor architecture, Register Set, Modes of operation and overview of Instructions

UNIT - IV

Interrupts & Device Drivers Exceptions and Interrupt handling Schemes – Context & Periods for Context Switching, Deadline & interrupt latency. Device driver using Interrupt Service Routine, Serial port Device Driver, Device drivers for Internal Programmable timing devices

UNIT - V

Network Protocols Serial communication protocols, Ethernet Protocol, SDMA, Channel & IDMA, External Bus Interface

TEXT BOOKS

 Embedded Systems - Architecture Programming and Design - Raj Kamal, 2nd ed., 2008,TMH.

2. PIC Microcontroller and Embedded Systems – Muhammad Ali Mazidi, Rolin D.Mckinaly, Danny Causy – PE.

3R C Designers Guide to the Cypress PSOC – Robert Ashpy, 2005, Elsevier.

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- 1. Embedded Microcomputer Systems, Real Time Interfacing Jonathan W. Valvano Brookes / Cole, 1999, Thomas Learning.
- 2. ARM Systems Developers Guides-Design & Optimizing System Software Andrew N. Sloss, Dominic Symes, Chris Wright, 2004, Elsevier.
- 3. Designing with PIC Microcontrollers- John B. Peatman, 1998, PH Inc.

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MEC1051: DIGITAL SIGNAL PROCESSORS AND ARCHITECTURE

Lecture

: 4 Periods/week

Internal Marks

: 40

External Marks

: 60

Credits

External Examination : 3 Hrs

UNIT - I

INTRODUCTION TO DIGITAL SIGNAL PROCESING

Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation, Analysis and Design tool for DSP Systems MATLAB, DSP using MATLAB.

COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS

Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT - II

ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES

Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT - III

EXECUTION CONTROL AND PIPELINING

Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.

PROGRAMMABLE DIGITAL SIGNAL PROCESSORS

Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

UNIT - IV

IMPLEMENTATIONS OF BASIC DSP ALGORITHMS

The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing.

IMPLEMENTATION OF FFT ALGORITHMS

An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XXI Computation of the signal spectrum.

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UNIT - V

INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA). A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

TEXT BOOKS

- 1. Digital Signal Processing Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
- 2. DSP Processor Fundamentals, Architectures & Features Lapsley et al. 2000, S. Chand & Co.

REFERENCES

1. Digital Signal Processors, Architecture, Programming and Applications – B. Venkataramani and M. Bhaskar, 2002, TMH.

2. Digital Signal Processing – Jonatham Stein, 2005, John Wiley.

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Communication Engineering

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MEC1052: IMAGE AND VIDEO PROCESSING

Lecture

: 4 Periods/week

Internal Marks

: 40

External Marks

: 60

Credits

External Examination

: 3 Hrs

UNIT - I

Fundamentals of Image Processing and Image Transforms

Basic steps of Image Processing System Sampling and Quantization of an image – Basic relationship between pixels Image Transforms: 2 D- Discrete Fourier Transform, Discrete Cosine Transform (DCT), Wavelet Transforms: Continuous Wavelet Transform, Discrete Wavelet Transforms.

UNIT - II

Image Processing Techniques - Image Enhancement Spatial domain methods:

Histogram processing, Fundamentals of Spatial filtering, Smoothing spatial filters, Sharpening spatial filters. Frequency domain methods: Basics of filtering in frequency domain, image smoothing, image sharpening, Selective filtering.

Image Segmentation

Segmentation concepts, Point, Line and Edge Detection, Thresholding, Region Based segmentation.

UNIT - III

Image Compression

Image compression fundamentals - Coding Redundancy, Spatial and Temporal redundancy, Compression models: Lossy& Lossless, Huffman coding, Arithmetic coding, LZW coding, Run length coding, Bit plane coding, Transform coding, Predictive coding, Wavelet coding, JPEG Standards.

UNIT - IV

Basic steps of Video Processing

Analog Video, Digital Video. Time-Varying Image Formation models: Three-Dimensional Motion Models, Geometric Image Formation, Photometric Image Formation, Sampling of Video signals, Filtering operations.

UNIT - V

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2-D Motion Estimation

Optical flow, General Methodologies, Pixel Based Motion Esimation, Block- Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Region based Motion Estimation, Multi resolution motion estimation, Waveform based coding, Block based transform coding, Predictive coding, Application of motion estimation in Video coding.

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TEXT BOOKS

1.

Digital Image Processing – Gonzaleze and Woods, 3 ded., Pearson. Video processing and communication – Yao Wang, JoemOstermann and Ya–quin Zhang. 1 Ed., PH Int. 2.

REFRENCES

Digital Video Processing - M. Tekalp, Prentice Hall International 1.

BRC

BARRA Department of Electronics & Communication Engineering Lakireddy Bali Reddy College of Engineering MYLAVARAM, Krishna Dt., Andhrapradesh. MEC1061: RADAR SIGNAL PROCESSING

Lecture

: 4 Periods/week

Internal Marks

: 40

External Marks

: 60

Credits

. 4

External Examination

: 3 Hrs

UNIT - I

Introduction— Radar Block Diagram, Radar Equation, Information Available from Radar Echo. Review of Radar Range Performance— General Radar Range Equation, Radar Detection with Noise Jamming, Beacon and Repeater Equations, Bistatic Radar.Matched Filter Receiver—Impulse Response, Frequency Response Characteristic and its Derivation, Matched Filter and Correlation Function, Correlation Detection and Cross-Correlation Receiver. Efficiency of Non-Matched Filters, Matched Filter for Non-White Noise.

UNIT - II

Detection of Radar Signals in Noise: Detection Criteria – Neyman-Pearson Observer, Likelihood-Ratio Receiver, Inverse Probability Receiver, Sequential Observer. Detectors – Envelope Detector, Logarithmic Detector, I/Q Detector. Automatic Detection -CFAR Receiver, Cell Averaging CFAR Receiver, CFAR Loss, CFAR Uses in Radar. Radar Signal Management – Schematics, Component Parts, Resources and Constraints.

UNIT - III

Waveform Selection [3, 2]: Radar Ambiguity Function and Ambiguity Diagram – Principles and Properties; Specific Cases – Ideal Case, Single Pulse of Sine Wave, Periodic Pulse Train, Single Linear FM Pulse, Noiselike Waveforms. Waveform Design Requirements.Optimum Waveforms for Detection in Clutter, Family of Radar Waveforms.

UNIT-IV

Pulse Compression in Radar Signals: Introduction, Significance, Types. Linear FM Pulse Compression – Block Diagram, Characteristics, Reduction of Time Sidelobes, Stretch Techniques, Generation and Decoding of FM Waveforms – Block Schematic and Characteristics of Passive System, Digital Compression, SAW Pulse Compression.

UNIT - V

Phase Coding Techniques: Principles, Binary Phase Coding, Barker Codes, Maximal Length Sequences (MLS/LRS/PN), Block Diagram of a Phase Coded CW Radar. Poly Phase Codes: Frank Codes, Costas Codes, Non-Linear FM Pulse Compression, Doppler Tolerant PC Waveforms – Short Pulse, Linear Period Modulation (LPM/HFM). Sidelobe Reduction for Phase Coded PC Signals.

TEXT BOOKS

1. Radar Handbook - M.I. Skolnik, 2nd ed., 1991, McGraw Hill.

BR Radar Design Principles: Signal Processing and The Environment - Fred E.

Nathanson,2 ed., 1999, PHI.

Introduction to Radar Systems - M.I. Skolnik, 3 ed., 2001, TMH.

Department of Electronics & Communication Engineering Lakireddy Bali Reddy College of Engineering MYLAVARAM, Krishna Dt., Andhrapradesh.

- 1. Radar Principles Peyton Z. Peebles, Jr., 2004, John Wiley.
- 2. Radar Signal Processing and Adaptive Systems R. Nitzberg, 1999, Artech House.
- 3. Radar Design Principles F.E. Nathanson, 1 ed., 1969, McGraw Hill.

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MEC1062: BIO-MEDICAL SIGNAL PROCESSING

Lecture

: 4 Periods/week

Internal Marks

: 40

External Marks

: 60

Credits

4

External Examination

: 3 Hrs

UNIT - I

Discrete and continuous Random variables, Probability distribution and density functions. Gaussian and Rayleigh density functions, Correlation between random variables. Stationary random process, Ergodicity, Power spectral density and autocorrelation function of random processes. Noise power spectral density analysis, Noise bandwidth, noise figure of systems.

UNIT-II

Data Compression Techniques: Lossy and Lossless data reduction Algorithms. ECG data compression using Turning point, AZTEC, CORTES, Huffman coding, vector quantisation, DCTand the K L transform.

UNIT-III

Cardiological Signal Processing: Pre-processing. QRS Detection Methods.Rhythm analysis.Arrhythmia Detection Algorithms.Automated ECG Analysis.ECG Pattern Recognition.Heart rate variability analysis. Adaptive Noise Cancelling: Principles of Adaptive Noise Cancelling. Adaptive Noise Cancelling with the LMS Adaptation Algorithm.Noise Cancelling Method to Enhance ECG Monitoring.Fetal ECG Monitoring.

UNIT-IV

Signal Averaging, polishing – mean and trend removal, Prony's method, Prony's Method based on the Least Squares Estimate, Linear prediction. Yule – walker (Y –W) equations, Analysis of Evoked Potentials.

UNIT-V

Neurological Signal Processing: Modeling of EEG Signals. Detection of spikes and spindles Detection of Alpha, Beta and Gamma Waves. Auto Regressive(A.R.) modeling of seizure EEG. Sleep Stage analysis. Inverse Filtering.Least squares and polynomial modeling.

TEXT BOOKS

Probability, Random Variables & Random Signal Principles – Peyton Z. Peebles, 4 ed., 2009, TMH.

Biomedical Signal Processing- Principles and Techniques - D.C.Reddy, 2005, TMH.

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Lakireddy Bali Reddy College of Engineering
MYLAVARAM, Krishna Dt., Andhrapradesh.

- 1. Digital Bio signal Processing Weitkunat R, 1991, Elsevier.
- 2. Biomedical Signal Processing Akay M, IEEE Press.
- 3. Biomedical Signal Processing -Vol. I Time & Frequency Analysis Cohen.A, 1986, CRC Press.

4. Biomedical digital Signal Processing : C-Language Experiments and Laboratory Experiments, willisJ.Tompkins, PHI.

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MEC152: ADVANCED DIGITAL SIGNAL PROCESSING LAB

Lecture : 3 Periods/week Internal Marks : 40

External Marks : 60

Credits : 2 External Examination : 3 Hrs

Cycle-1 SIGNALS & SYSTEM

- 1. Signal Classifications And Properties
- 2. Convolution
- 3. Correlation and Covariance of a Random Signal
- 4. Discrete Fourier Transform
- 5. Data Acquisition of Audio Signal using MATLAB

Cycle-2 FILTERS

- 6. Analog Filters
- 7. Digital Filters

Cycle-3 SPECTRAL ESTIMATION

- 8. Periodogram Based methods
- 9. Parametric Methods

Cycle-4 MULTIRATE SIGNAL PROCESSING

- 10. Decimation
- 11. Interpolation

Cycle-5 ADAPTIVE FILTERING

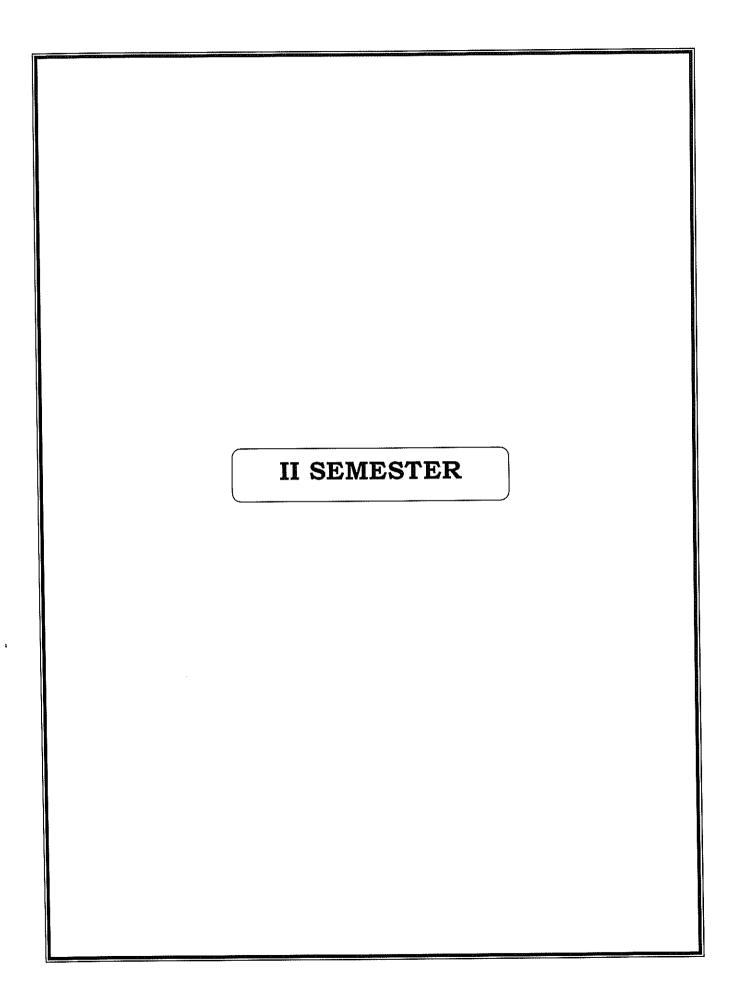
- 12. Least Mean Square Algorithm
- 13. Recursive Least Squares
- 14. Wiener Filter

Cycle-6 APPLICATIONS

- 15. Average Energy Calculation
- 16. Effect of Window Length
- 17. Voiced or Unvoiced Detection
- 18. Pitch calculation
- 19. Spectral Subtraction method for Speech enhancement



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MEC201: ADAPTIVE SIGNAL PROCESSING

Lecture

: 4 Periods/week

Internal Marks

: 40

External Marks

: 60

Credits

External Examination

: 3 Hrs

UNIT - I

Introduction to Adaptive Systems Adaptive Systems: Definitions, Characteristics, Applications, Example of an Adaptive System. The Adaptive Linear Combiner - Description. Weight Vectors, Desired Response Performance function -Gradient & Mean Square Error.

UNIT - II

Development of Adaptive Filter Theory & Searching the Performance surface: Introduction to Filtering - Smoothing and Prediction - Linear Optimum Filtering, Problem statement, Principle of Orthogonality - Minimum Mean Square Error, Wiener- Hopf equations, Error Performance - Minimum Mean Square Error.

Searching the performance surface - Methods & Ideas of Gradient Search methods -Gradient Searching Algorithm & its Solution - Stability & Rate of convergence - Learning Curves.

UNIT - III

Steepest Descent Algorithms

Gradient Search by Newton's Method, Method of Steepest Descent, Comparison of Learning Curves.

UNIT - IV

LMS Algorithm & Applications

Overview - LMS Adaptation algorithms, Stability & Performance analysis of LMS Algorithms -LMS Gradient & Stochastic algorithms - Convergence of LMS algorithm. Applications: Noise cancellation - Cancellation of Echoes in long distance telephone circuits, Adaptive Beam forming.

UNIT - V

Kalman filtering:

Introduction - Recursive Mean Square Estimation Random variables, Statement of Kalman filtering problem - Filtering -Initial conditions - Variants of Kalman filtering - Extend Kalman filtering.

TEXT BOOKS

- Adaptive Signal Processing Bernard Widrow, Samuel D.Streams, 2005, PE. 1.
- 2. Adaptive Filter Theory - Simon Haykin-, 4 ed., 2002, PE Asia.

REFERENCES

LBR Optimum signal processing: An introduction - Sophocles. J. Orfamadis, 2 ed., 1988, McGraw-Hill, Newyork.

Adaptive signal processing-Theory and Applications, S.Thomas Alexander Springer -Verlag.

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M.TECH (SYSTEMS AND SIGNAL PROCESSING), A.Y.2010-2011

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MEC202: SPEECH PROCESSING

Lecture : 4 Periods/week

Internal Marks

: 40

External Marks

: 60

Credits :

External Examination

: 3 Hrs

UNIT - I

Fundamentals of Digital Speech Processing: Anatomy & Physiology of Speech Organs, The process of Speech Production, The Acoustic Theory of Speech Production, Digital models for speech signals.

UNIT-II

Time Domain Models for Speech Processing

Introduction- Window considerations, Short time energy and average magnitude Short time average zero crossing rate ,Speech vs. silence discrimination using energy and zero crossing, Pitch period estimation using a parallel processing approach, The short time autocorrelation function, The short time average magnitude difference function, Pitch period estimation using the autocorrelation function.

UNIT - III

Linear predictive coding (LPC) analysis

Basic principles of Linear Predictive Analysis:The Autocorrelation Method, The Covariance Method, Solution of Lpc Equations: Cholesky Decomposition Solution for Covariance Method, Durbin's Recursive Solution for the AutoCorrelation Equations, Comparision between the Methods of Solution of the LPC Analysis Equations, Applications of LPC Parameters: Pitch Detection using LPC Parameters, Formant Analysis using LPC Parameters.

Homomorphic Speech Processing

Introduction, Homomorphic Systems for Convolution: Properties of the Complex Cepstrum, Computational Considerations, The Complex Cepstrum of Speech, Pitch Detection, Formant Estimation, The HomomorphicVocoder.

UNIT - IV

Speech enhancement: -Nature of interfering sounds, Speech enhancment techniques: Single Microphone Approach: spectral substraction, Enhancement by re-synthesis, Comb filter, Wiener filter, Multimicrophone Approach.

Automatic speech recognition-Basic pattern recognition approaches, Parametric represention of speech, Evaluating the similarity of speech patterns, Isolated digit Recognition System,.Contineous digit Recognition System

UNIT-V

Hidden Markov Model (HMM) for Speech

Hidden markov model (HMM) for speech recognition, Viterbialgorithm, Training and testing using HMMS, Adapting to variability in speech (DTW), Language models.

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Speaker recognition

Recognition techniques, Features that distinguish speakers, Speaker Recognition Systems: Speaker Verification System, Speaker Identification System.

TEXT BOOKS

- 1. Digital processing of speech signals L.R Rabiner and S.W.Schafer. Pearson Education.
- 2. Speech Communications : Human & Machine Douglas O'Shaughnessy, 2 ed., IEEE Press.
- 3. Digital processing of speech signals. L.R Rabinar and R W Schafer,1978, PHI.

REFERENCES

- 1. Discrete Time Speech Signal Processing : principles and Practice Thomas F. Quateri 1 ed., PE.
- 2. Speech & Audio Signal Processing- Ben Gold & Nelson Morgan, 1 ed., Wiley.

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Department of Electronics & Communication Engineering Lakireddy Bali Reddy College of Engineering MYLAVARAM, Krishna Dt., Andhrapradesh.

MEC203: SOC ARCHITECTURE

Lecture

: 4 Periods/week

Internal Marks

: 40

External Marks

: 60

Credits

. 4

External Examination

: 3 Hrs

UNIT - I

Introduction to Processor Design:

Abstraction in Hardware Design, MUO a simple processor, Processor design trade off, Design for low power consumption.

ARM Processor as System-on-Chip: Acorn RISC Machine – Architecture inheritance – ARM programming model – ARM development tools – 3 and 5 stage pipeline ARM organization – ARM instruction execution and implementation – ARM Co-processor interface

UNIT - II

ARM Assembly Language Programming:

ARM instruction types – data transfer, data processing and control flow instructions – ARM instruction set – Co-processor instructions.

Architectural Support for High Level Language: Data types – abstraction in Software design – Expressions – Loops – Functions and Procedures – Conditional Statements – Use of Memory

UNIT - III

Memory Hierarchy: Memory size and speed – On-chip memory – Caches – Cache designan example – memory management

UNIT - IV

Architectural Support for System Development: Advanced Microcontroller bus architecture – ARM memory interface – ARM reference peripheral specification – Hardware system prototyping tools – Armulator – Debug architecture

UNIT - V

Architectural Support for Operating System: An introduction to Operating Systems – ARM system control coprocessor – CP15 protection unit registers – ARM protection unit – CP15 MMU registers – ARM MMU Architecture – Synchronization – Context Switching input and output

and output

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TEXT BOOKS

- 1. ARM System on Chip Architecture Steve Furber– 2nd ed., 2000, Addison Wesley Professional.
- Design of System on a Chip: Devices and Components Ricardo Reis, 1st ed., 2004, Springer

REFERENCES

1. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM System on Chip Verification – Methodologies and Techniques –PrakashRashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.



Department of Electronics & Communication Engineering Communication Engineering Eakireddy Bali Reddy College of Engineering MYLAVARAM, Krishna Dt., Andhrapradesh, MYLAVARAM, Krishna Dt., Andhrapradesh,

MEC204: CODING THEORY AND TECHNIQUES

Lecture

: 4 Periods/week

Internal Marks

: 40

External Marks

: 60

Credits

External Examination

: 3 Hrs

UNIT - I

Coding for Reliable Digital Transmission and storage: Mathematical model of Information, A Logarithmic Measure of Information, Average and Mutual Information and Entropy, Types of Errors, Error Control Strategies, Linear Block Codes; Introduction to Linear Block Codes, Syndrome and Error Detection, Minimum Distance of a Block code, Error-Detecting and Error-correcting Capabilities of a Block code, Standard array and Syndrome Decoding, Probability of an undetected error for Linear Codes over a BSC, Hamming Codes. Applications of Block codes for Error control in data storage system

UNIT-II

Cyclic codes: Description, Generator and Parity-check Matrices, Encoding, Syndrome Computation and Error Detection, Decoding ,Cyclic Hamming Codes, Shortened cyclic codes, Error-trapping decoding for cyclic codes, Majority logic decoding for cyclic codes.

UNIT- III

Convolutional codes: Encoding of Convolutional Codes, Structural and Distance Properties, maximum likelihood decoding, Sequential decoding, Majority- logic decoding of Convolution codes. Application of Viterbi Decoding and Sequential Decoding, Applications of Convolutional codes in ARQ system.

UNIT-IV

Burst -Error-Correcting codes: Decoding of Signle-Burst error Correcting Cyclic codes, Single-Burst-Error-Correcting Cyclic codes, Burst-Error-Correcting Convoulutional Codes, Bounds on Burst Error-Correcting Capability, Interleaved Cyclic and Convolutional Codes, Phased-Burst - Error-Correcting Cyclic and Convolutional codes.

UNIT - V

BCH - Codes: BCH code- Definition, Minimum distance and BCH Bounds, Decoding Procedure for BCH Codes-Syndrome Computation and Iterative Algorithms, Error Location Polynomials and Numbers for single and double error correction

TEXT BOOKS

Error Control Coding-Fundamentals and Applications -Shu Lin, Daniel J.Costello, Jr, Prentice Hall, Inc.

Erro Correcting Coding Theory-Man Young Rhee- 1989, McGraw-Hill Publishing

Department of Electronics & Communication Engineering Lakireddy Bali Reddy College of Engineering MYLAVARAM Krishna Dt., Andhrapradesh

- Digital Communications-Fundamental and Application Bernard Sklar, PE.
- 2. Digital Communications- John G. Proakis, 5th ed., 2008, TMH.
- 3. Introduction to Error Control Codes-Salvatore Gravano-oxford
- 4. Error Correction Coding Mathematical Methods and Algorithms Todd K.Moon, 2006, Wiley India.

5. Information Theory, Coding and Cryptography – Ranjan Bose, 2 Edition, 2009, TMH.

HEAD

Department of Electronics & Communication Engineering Lakireddy Bali Reddy College of Engineering MYLAVARAM Krishna Dt., Andhrapradesh.

MEC2051: CPLD & FPGA ARCHITECTURES AND APPLICATIONS

Lecture : 4 Periods/week Internal Marks

External Marks

: 60

Credits

External Examination

: 3 Hrs

UNIT - I

Programmable logic: ROM, PLA, PAL PLD, PGA - Features, programming and applications using complex programmable logic devices Altera series - Max 5000/7000 series and Altera FLEX logic-10000 series CPLD, AMD's- CPLD (Mach 1to 5), Cypres FLASH 370 Device technology, Lattice PLST's architectures - 3000 series - Speed performance and in system programmability.

UNIT - II

FPGAs: Field Programmable gate arrays- Logic blocks, routing architecture, design flow technology mapping ifor FPGAs, Case studies Xitir x XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT &T ORCA's (Optimized Reconfigurable Cell Array): ACTEL's ACT-1,2,3 and their speed performance

UNIT - III

Alternative realization for state machine chat suing microprogramming linked state machine one -hot state machine, petrinetes for state machines-basic concepts, properties, extended petrinetes for parallel controllers.

UNIT - IV

Digital front end digital design tools for FPGAs& ASICs: Using mentor graphics EDA tool ("FPGA Advantage") - Design flow using FPGAs

UNIT - V

Case studies of paraller adder cell paraller adder sequential circuits, counters, multiplexers, parellel controllers.

TEXT BOOKS

1. Field Programmable Gate Array Technology - S. Trimberger, Edr, 1994, Kluwer Academic Publications.

2. Field Programmable Gate Arrays, John V.Oldfield, Richard C Dore, Wiley

Bublications.

Department of Electronics & Communication Engineering

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- 1. Digital Design Using Field Programmable Gate Array, P.K.Chan & S. Mourad, 1994, Prentice Hall.
- Digital System Design using Programmable Logic Devices Parag.K.Lala, 2003, BSP.
- 3. Field programmable gate array, S. Brown, R.J.Francis, J.Rose, Z.G.Vranesic, 2007, BSP.

4. Digital Systems Design with FPGA's and CPLDs – Ian Grout, 2009, Elsevier

ROUNDS

Department of Electronics & Communication Engineering Lakireddy Bali Reddy College of Engineering MYLAVARAM, Krishna Dt., Andhrapradesh

MEC2052: DESIGN FOR TESTABILITY

Lecture

: 4 Periods/week

Internal Marks

: 40

External Marks

: 60

Credits

: 4

External Examination

: 3 Hrs

UNIT - I

Introduction to Test and Design for Testability (DFT) Fundamentals

Modeling: Modeling Digital Circuits at Logic Level, register Level, and Structural Models. Levels of Modeling, Logic Simulation: Types of Simulation, Delay Models, Element Evaluation, Hazard Detection, Gate Level Event Driven Simulation.

<u>UNIT – II</u>

Fault Modeling: Logic Fault Models, Fault Detection and Redundancy, Fault equivalence and Fault Location. Single Stuck and Multiple Stuck- Fault Models. Fault Simulation Applications, General Techniques for Combinational Circuits.

UNIT - III

Testing for Single Stuck Faults (SSF) – Automated Test Pattern Generation(ATPG/ATG) for SSFs in Combinational and Sequential Circuits, Functional Testing with Specific Fault Models, Vector Simulation - ATPG Vectors, Formats, Compaction and Compression, Selecting ATPG Tool.

UNIT - IV

Design for Testability - testability Trade-off's Techniques, Scan Architectures and Testing, Controllability and Absorbability, Generic Boundary Scan, Full Integrated Scan, Storage Cells foe Scan Design, Board level and System level approaches, Boundary Scans Standards, Compression Techniques - Different Techniques, Syndrome test and Signature analysis.

UNIT - V

Built-in Self test (BIST) - BIST Concepts and Test pattern Generation. Specific BIST Architectures - LOCST, STUMPS, CBIST, RTD, BILBO. Brief ideas on some advanced BIST concepts and design for self-test at board level. Memory BIST (MBIST): Memory Test Architectures and Techniques, Introduction to Memory Test, Types of Memories and Integration, Embedded Memory Testing Model, Memory Test requirements for MBIST, JTAG Testing Features.

TEXT BOOKS

- 1. Digital Systems Testing and Testable Design - MironAbramovici, Melvin A. Breur, ArthuD.Friedman, John Wiley & Sons.
- Design for Test for Digital ICs & Embedded Core Systems Alfred Crouch, 2008, 2.
- B Introduction to VLSI Testing Robrt.J.Feugate J, Steven M.McIntyre, Englehood Cliffs, 1988, Prentice Hall.

REFERENCES

Essentials of Electronic Testing - M.L. Bushnell, Vishwani.D.Agarwal, Sprin

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MEC2061: WIRELESS COMMUNICATION AND NETWORKS

Lecture : 4 Periods/week Internal Marks

al Marks : 40

External Marks

: 60

Credits :

External Examination

: 3 Hrs

UNIT - I

Wireless Communications & System Fundamentals: Introduction to wireless communications systems, examples, comparisons & trends, Cellular concepts-frequency reuse, strategies, interference & system capacity, trucking & grade of service, improving coverage &capacity in cellular systems.

UNIT - II

Multiple Access Techniques for Wireless Communication: FDMA, TDMA, SSMA (FHMA/CDMA/Hybrid techniques), SDMA technique (AS applicable to wireless communications). Packet radio access-protocols, CSMA protocols, reservation protocols, capture effect in packet radio, capacity of cellular systems.

UNIT - III

Wireless Networking: Introduction, differences in wireless & fixed telephone networks, traffic routing in wireless networks – circuit switching, packet switching X.25 protocol. Wireless data services – cellular digital packet data (CDPD), advanced radio data information systems, RAM mobile data (RMD). Common channel signaling (CCS), ISDN-Broad band ISDN & ATM, Signaling System no .7 (SS7)-protocols, network services part, user part, signaling traffic, services & performance

UNIT-IV

Mobile IP and Wireless Application Protocol: Mobile IP Operation of mobile IP, Colocated address, Registration, Tunneling, WAP Architecture, overview, WML scripts, WAP service, WAP session protocol, wireless transaction, Wireless datagram protocol. Wireless LAN Technology, Infrared LANs, Spread spectrum LANs, Narrow bank microwave LANs, IEEE 802 protocol Architecture, IEEE802 architecture and services, 802.11 medium access control, 802.11 physical layer.

UNIT - V

Mobile Data Networks: Introduction, Data oriented CDPD Network, GPRS and higher data rates, Short messaging service in GSM, Mobile application protocol. Ad-hoc Wireless Networks: Cellular and Adhoc wireless networks, applications, MAC protocols, Routing, Multicasting, Transport layer Protocols, quality of service browsing, deployment considerations, Adhoc wireless Internet

TEXT BOOKS

1. Wireless Communication and Networking - William Stallings, 2003, PHI.

2 Wireless Communications, Principles, Practice-Theodore, S.Rappaport, 2 Ed. 2002, PHI.

3. Principles of Wireless Networks – Kaveh Pah Laven and P. Krishna Murthy, 2002, Rearson Education publishers

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1. Wireless Digital Communications – Kamilo Feher, 1999, PHI.

2. Telecommunication System Engineering – Roger L. Freeman, 4/ed., Wiley-Interscience, John Wiley & Sons, 2004.

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MEC2062: VLSI SIGNAL PROCESSING

Lecture

: 4 Periods/week

Internal Marks

: 40

External Marks

: 60

Credits

: 4

External Examination

: 3 Hrs

UNIT - I

Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power Retiming: Introduction – Definitions and Properties – Solving System of Inequalities – Retiming Techniques

UNIT - II

Folding and Unfolding: Folding: Introduction -Folding Transform - Register minimization Techniques - Register minimization in folded architectures - folding of multirate systems **Unfolding:** Introduction - An Algorithm for Unfolding - Properties of Unfolding - critical Path, Unfolding and Retiming - Applications of Unfolding

UNIT - III

Systolic Architecture Design: Introduction – Systolic Array Design Methodology – FIR Systolic Arrays – Selection of Scheduling Vector – Matrix Multiplication and 2D Systolic Array Design – Systolic Design for Space Representations contain Delays

UNIT - IV

Fast Convolution: Introduction – Cook-Toom Algorithm – Winogard algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

UNIT - V

Low Power Design: Scaling Vs Power Consumption –Power Analysis, Power Reduction techniques – Power Estimation Approaches Programmable DSP: Evaluation of Programmable Digital Signal Processors, DSP Processors for Mobile and Wireless Communications, Processors for Multimedia Signal Processing

TEXT BOOKS

- 1. VLSI Digital Signal Processing- System Design and Implementation Keshab K. Parthi, 1998, Wiley Inter Science.
- 2. VLSI and Modern Signal processing Kung S. Y, H. J. While House, T. Kailath, 1985, Prentice Hall.

REFERENCES

1. Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing – Jose E. France, YannisTsividis, 1994, Prentice Hall.

VLSI Digital Signal Processing – Medisetti V. K ,1995, IEEE Press (NY), USA

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M.TECH (SYSTEMS AND SIGNAL PROCESSING), A.Y.2010-2011

MEC208: ADVANCED ECAD LAB

Lecture

: 3 Periods/week

Internal Marks

: 40

External Marks

: 60

Credits

: 2

External Examination

: 3 Hrs

LIST OF EXPERIMENTS

Design FULL ADDER using verilog HDL and implementation on Sparten3E

1. FULL ADDER

2. MULTIPLEXER

3. PARALLEL ADDER

4. Combinational Multiplier

5. ALU

6. Counter

7. Linear feedback Shift Register

8. Decade Counter

9. 3-STAGE Decade Counter

10. Binary Multiplier

11. Digital Clock

12. DICE GAME



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Lakireddy Ram Norman Jt. Andreas